

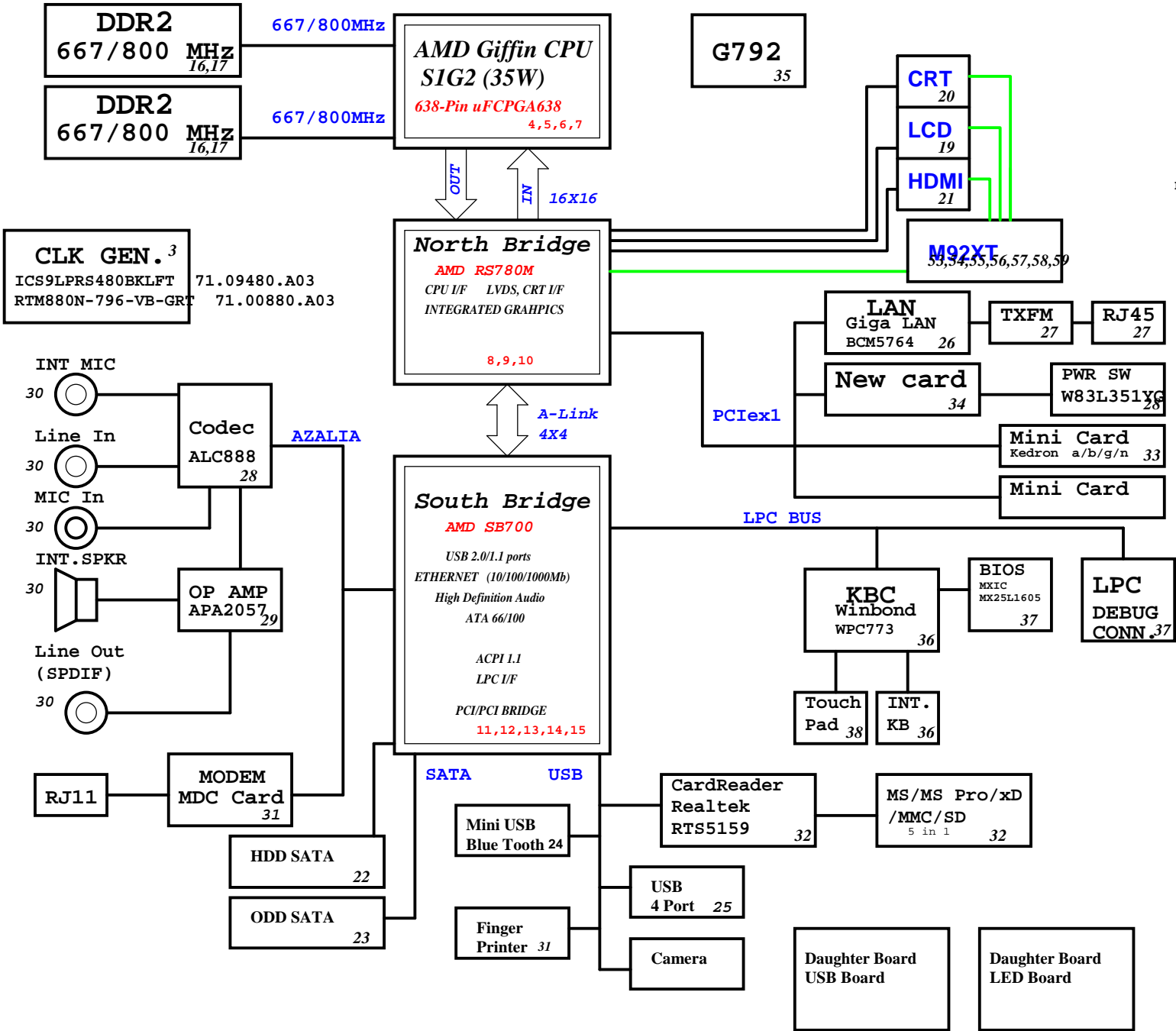
JV50-PU Block Diagram

Project code: 91.4CH01.001
PCB P/N : 48.4C901.001
REVISION :08252- -SB

PCB STACKUP

TOP	_____
VCC	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

SYSTEM DC/DC	
ISL62392HR	46
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A)
	3D3V_S5(6A)
SYSTEM DC/DC	
TPS51124	47
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A)
	1D2V_S0(4A)
SYSTEM DC/DC	
RT8202	49
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)
RT9025	
49	
5V_S5	1D1V_M92
RT9161	
49	
3D3V_S0	2D5V_S0(200mA)
G957	
49	
3D3V_S0	1D5V_S0(1A)
G9161	
49	
3D3V_S5	1D2V_S5(400mA)
CHARGER	
MAX8731	50
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	18V 6.0A
	UP+5V
	5V 100mA
CPU DC/DC	
ISL6265HR	45
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0
	0~1.55V 18A
	VCC_CORE_S0_1
	0~1.55V 18A
	VDDNB
	0~1.55V 18A





<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB/PCIE Routing

Size
A3

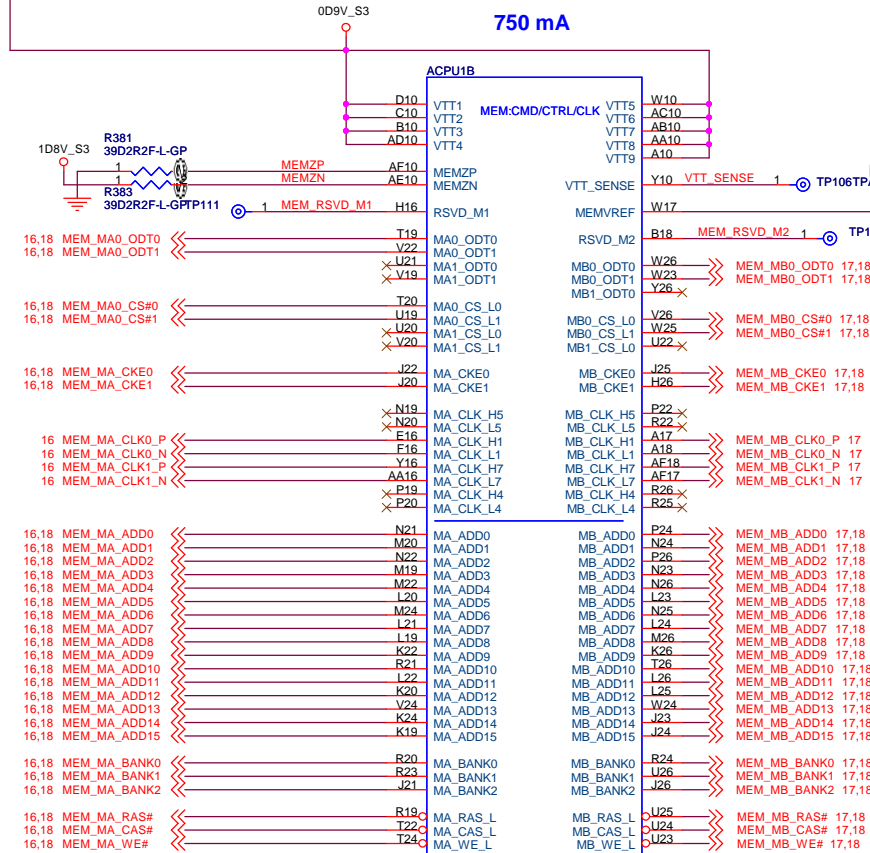
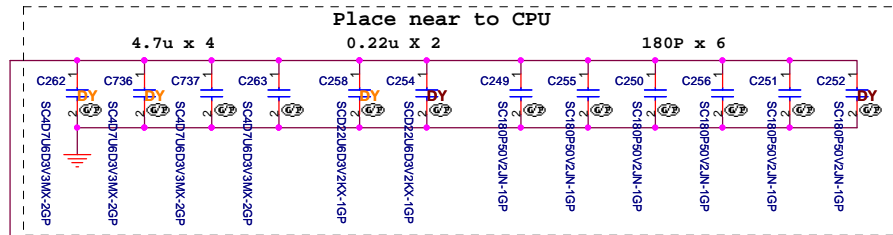
Document Number

JV50-PU

Rev
SB

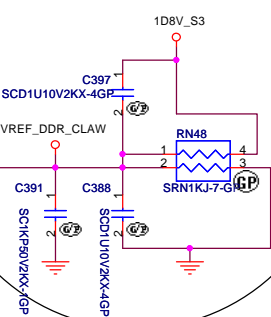
Date: Friday, December 19, 2008

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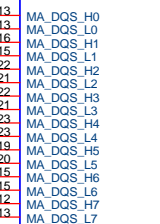
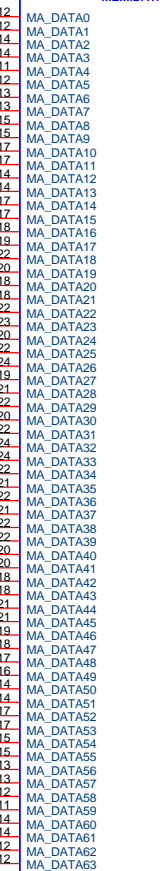


SKT-CPU638P-GP-U2

CLOSE TO CPU



ACPU1C

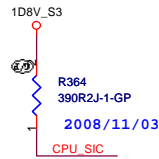
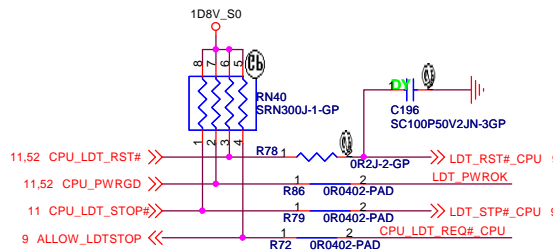


SKT-CPU638P-GP-U2

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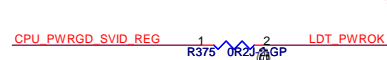
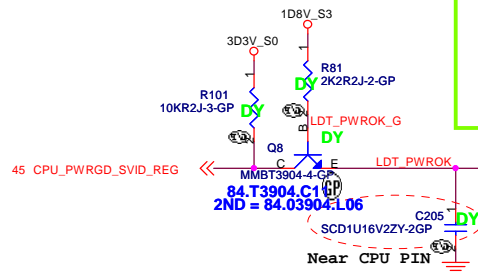
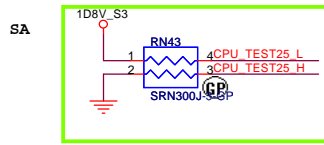
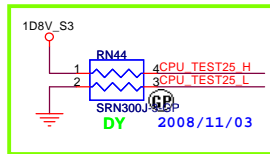
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU DDR (2/4)	
Size	Document Number	Rev	SB
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Date:	Friday, December 19, 2008	Sheet	5 of 61

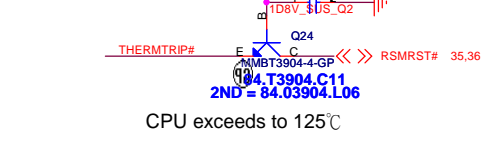
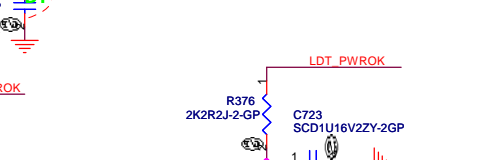
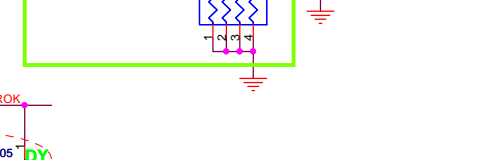
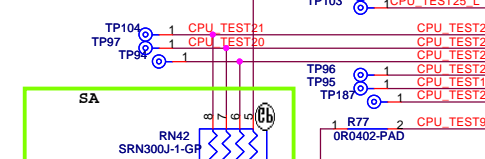
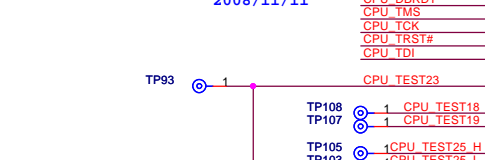
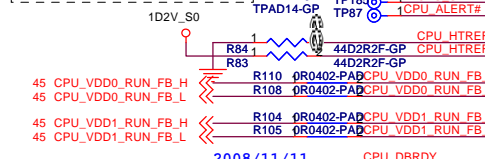
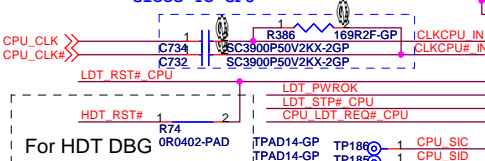
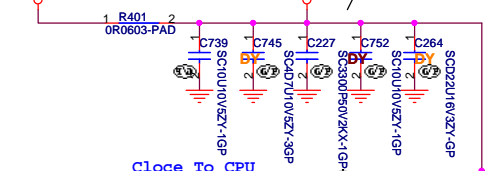


For leverage Slg3, please reserve 300 ohm resistor pullup to VDDIO.

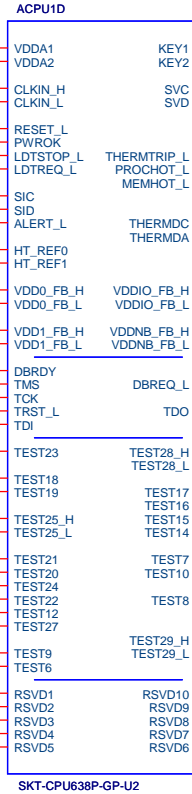
For leverage Slg3, please reserve 300 ohm resistor pulldown to VSS



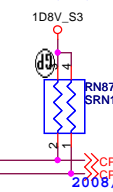
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



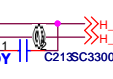
CPU exceeds to 125°C



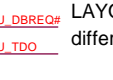
2008/11/03



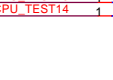
2008/11/05



2008/11/03



2008/11/03



2008/11/03



2008/11/03



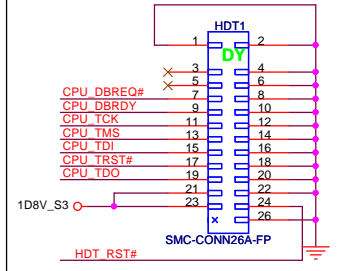
2008/11/03



2008/11/03

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

HDT Connectors



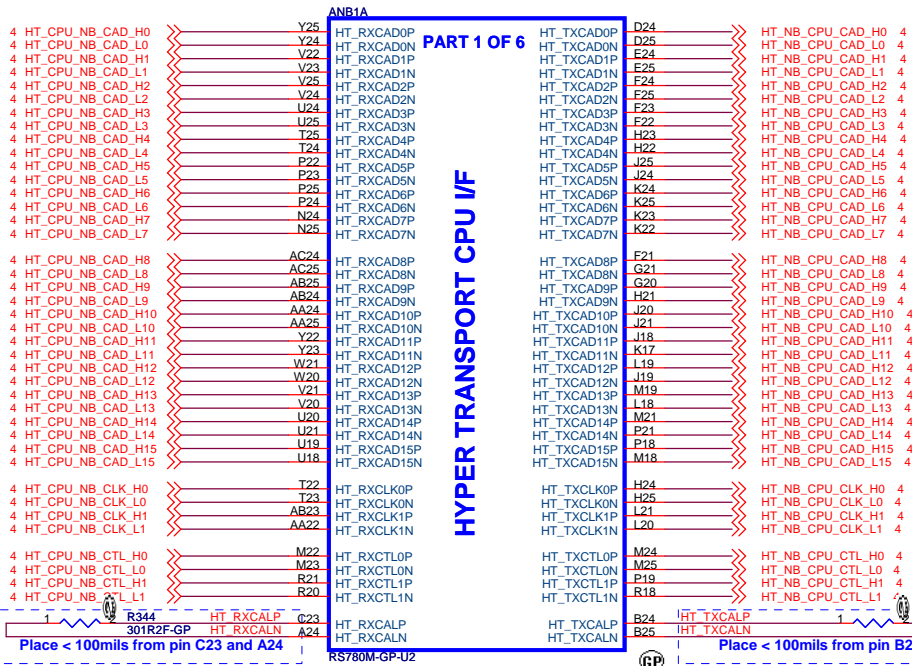
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Title: **CPU_Control&Debug (3/4)**

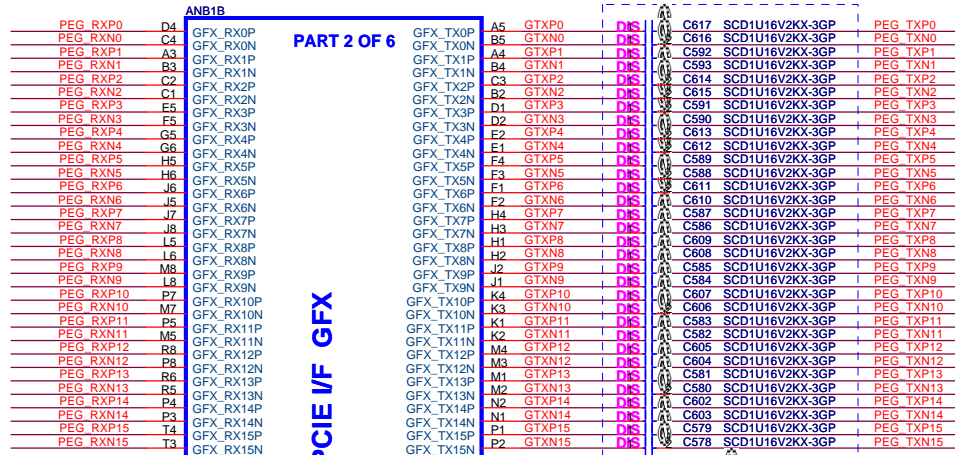
Size: **A3** Document Number: **JV50-PU** Rev: **SB**

Date: **Friday, December 19, 2008** Sheet: **6** of **61**



Placement: close RS780

Placement: close RS780



PEG_TXP1[15.0] 53
PEG_TXN[15.0] 53

RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

GTXP0	UMA	C30	1	SCD1U16V2KX-3GP	HDMI_DATA2+ 21
GTXP1	UMA	C29	1	SCD1U16V2KX-3GP	HDMI_DATA2- 21
GTXP2	UMA	C27	1	SCD1U16V2KX-3GP	HDMI_DATA1+ 21
GTXP3	UMA	C26	1	SCD1U16V2KX-3GP	HDMI_DATA1- 21
GTXP4	UMA	C25	1	SCD1U16V2KX-3GP	HDMI_DATA0+ 21
GTXP5	UMA	C22	1	SCD1U16V2KX-3GP	HDMI_DATA0- 21
GTXP6	UMA	C21	1	SCD1U16V2KX-3GP	HDMI_CLK+ 21
GTXP7	UMA	C19	1	SCD1U16V2KX-3GP	HDMI_CLK- 21

LAN 2008/11/05
MINICARD1 2008/11/05
MINICARD2 2008/11/05
NEW CARD

A-LINK

TPAD14-GP
TPAD14-GP

11 ALINK_NBRX_SBTX_P0
11 ALINK_NBRX_SBTX_N0
11 ALINK_NBRX_SBTX_P1
11 ALINK_NBRX_SBTX_N1
11 ALINK_NBRX_SBTX_P2
11 ALINK_NBRX_SBTX_N2
11 ALINK_NBRX_SBTX_P3
11 ALINK_NBRX_SBTX_N3

PCIE_RXP0
PCIE_RXN0
PCIE_RXP1
PCIE_RXN1
PCIE_RXP2
PCIE_RXN2
PCIE_RXP3
PCIE_RXN3
PCIE_RXP4
PCIE_RXN4
PCIE_RXP5
PCIE_RXN5

PCIE I/F GPP

PCIE I/F SB

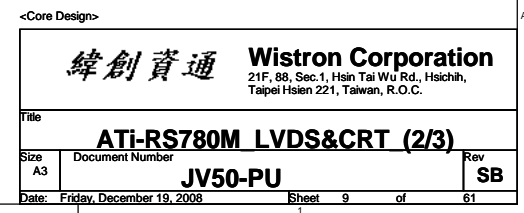
PCE_CALRP
PCE_CALRN

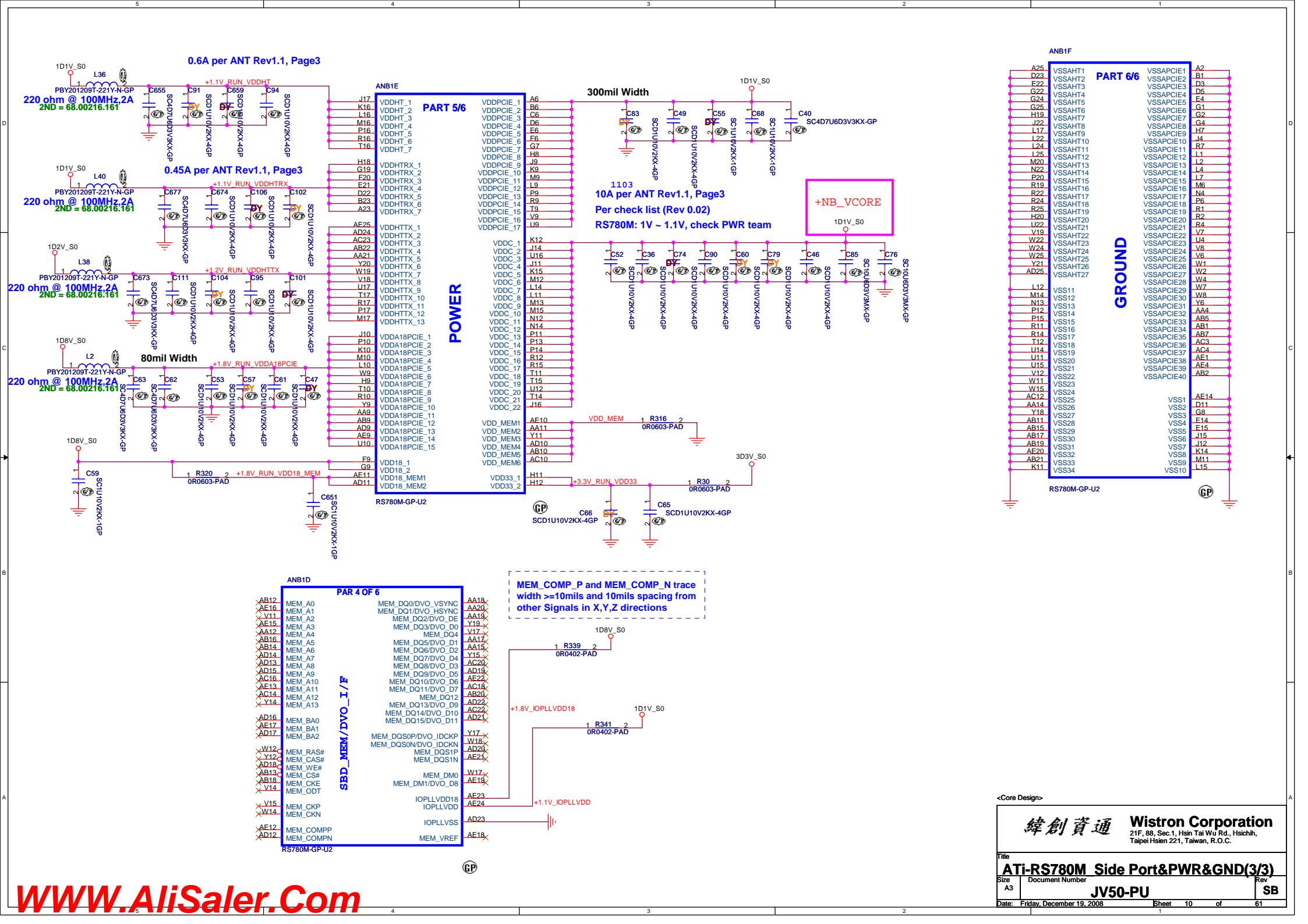
Place < 100mils from pin AC8 and AB8

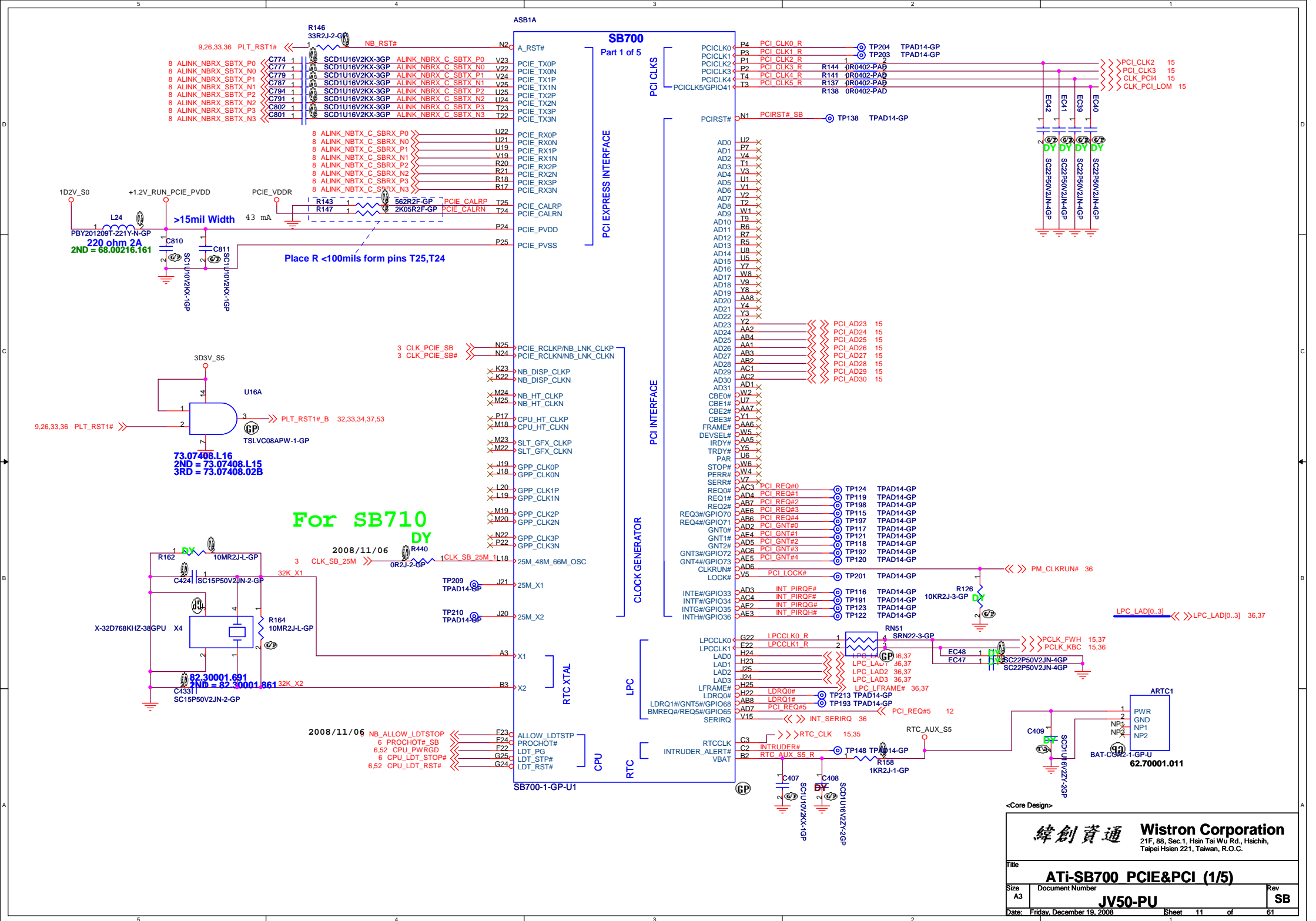
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Taipai Hsien 221, Taiwan, R.O.C.

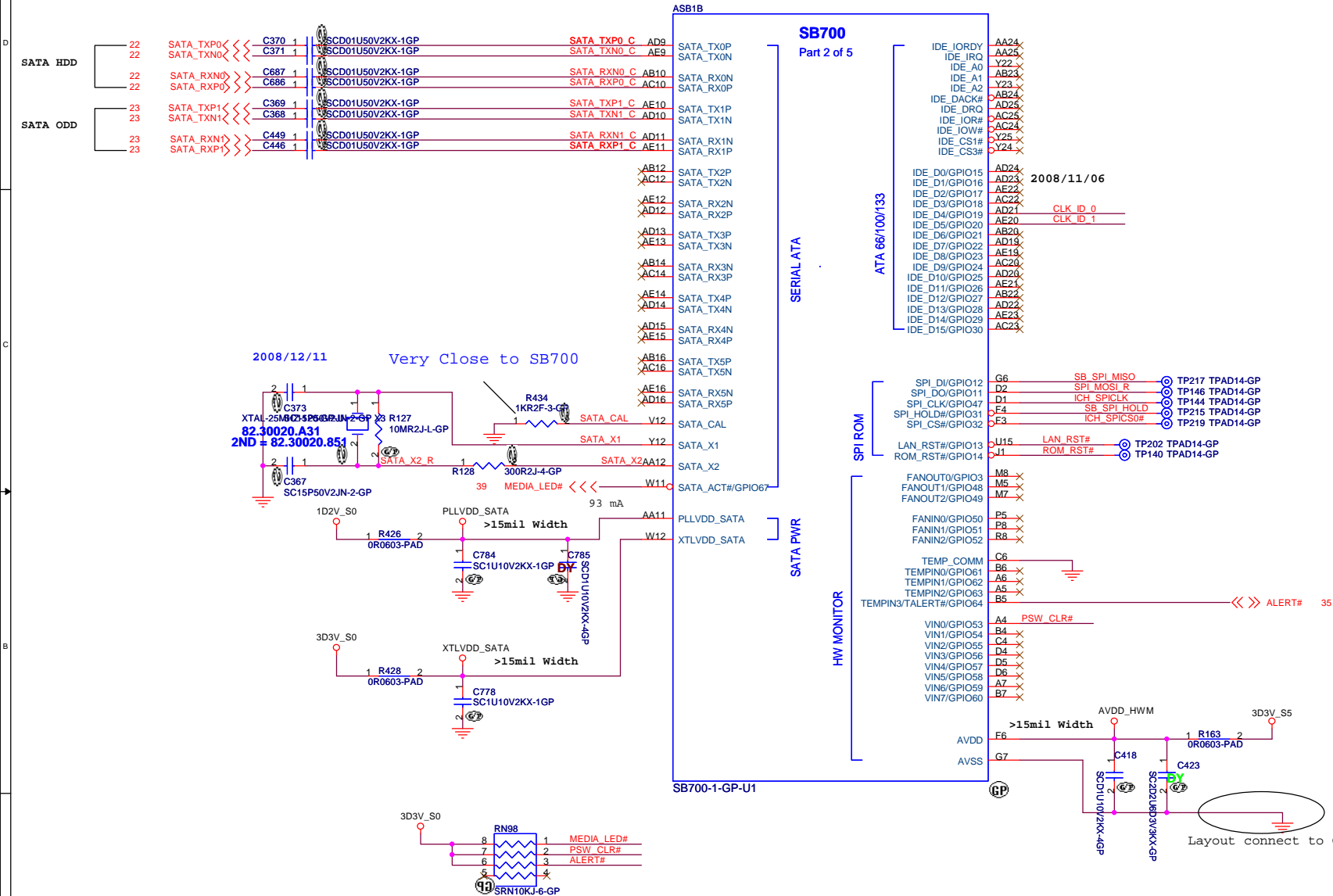
Title				ATI-RS780M_HT LINK&PCIe(1/3)	
Size	Document Number			Rev	
A3	JV50-PU			SB	
Date:	Friday, December 19, 2008			Sheet	8 of 61



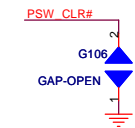
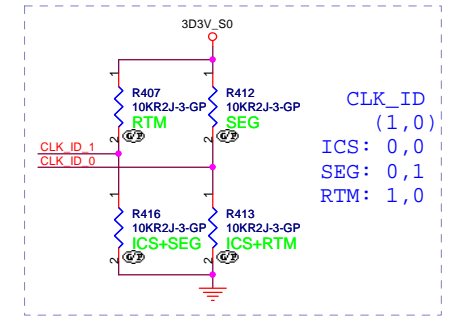




PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700



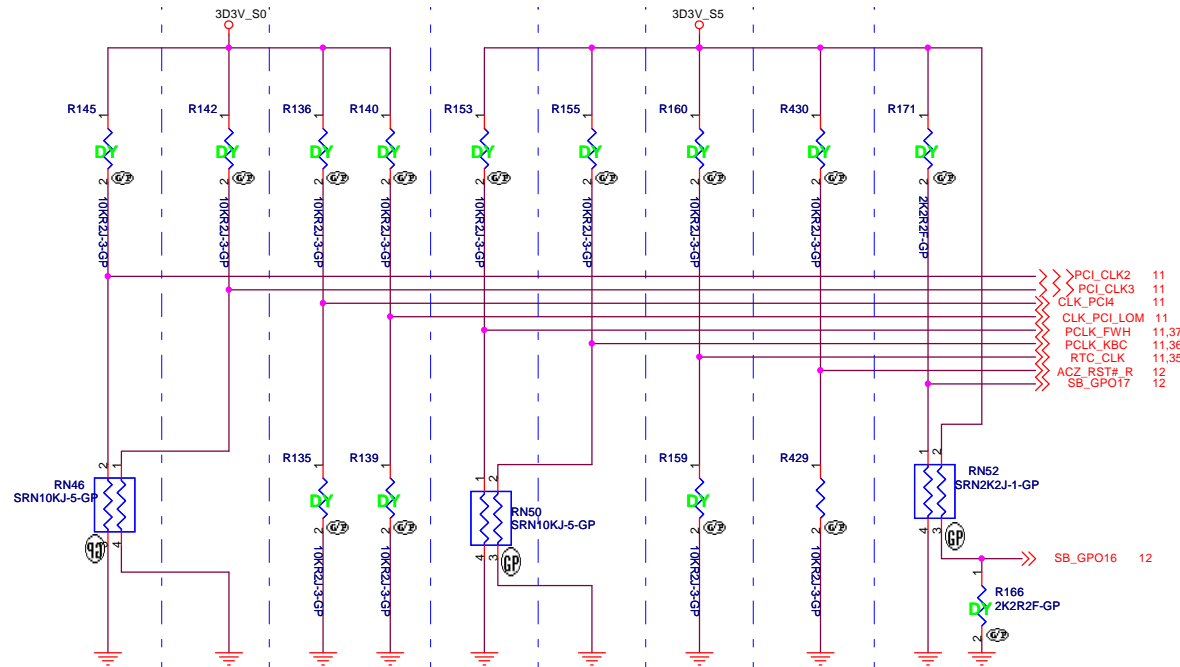
Dummy CKG select



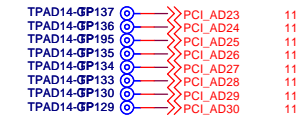
Layout connect to Cap then GND

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

ATI-SB700 STRAPPING (5/5)

Size

Document Number

A3

JV50-PU

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Rev

SB

5,18 MEM_MA_ADD0 >> 102 A0
5,18 MEM_MA_ADD1 >> 101 A1
5,18 MEM_MA_ADD2 >> 100 A2
5,18 MEM_MA_ADD3 >> 99 A3
5,18 MEM_MA_ADD4 >> 98 A4
5,18 MEM_MA_ADD5 >> 97 A5
5,18 MEM_MA_ADD6 >> 96 A6
5,18 MEM_MA_ADD7 >> 95 A7
5,18 MEM_MA_ADD8 >> 94 A8
5,18 MEM_MA_ADD9 >> 93 A9
5,18 MEM_MA_ADD10 >> 92 A10/AP
5,18 MEM_MA_ADD11 >> 91 A11
5,18 MEM_MA_ADD12 >> 90 A12
5,18 MEM_MA_ADD13 >> 89 A13
5,18 MEM_MA_ADD14 >> 88 A14
5,18 MEM_MA_ADD15 >> 87 A15
5,18 MEM_MA_BANK2 >> 107 BA0
5,18 MEM_MA_BANK0 >> 106 BA1
5,18 MEM_MA_BANK1 >> 105

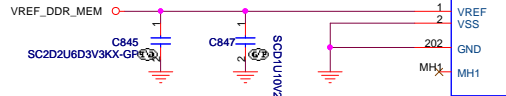
5,18 MEM_MA_BANK2 >> 107 BA0
5,18 MEM_MA_BANK0 >> 106 BA1
5,18 MEM_MA_BANK1 >> 105

5 MEM_MA_DATA0 >> 5 DQ0
5 MEM_MA_DATA1 >> 17 DQ1
5 MEM_MA_DATA2 >> 19 DQ2
5 MEM_MA_DATA3 >> 4 DQ3
5 MEM_MA_DATA4 >> 6 DQ4
5 MEM_MA_DATA5 >> 14 DQ5
5 MEM_MA_DATA6 >> 16 DQ6
5 MEM_MA_DATA7 >> 23 DQ7
5 MEM_MA_DATA8 >> 25 DQ8
5 MEM_MA_DATA9 >> 36 DQ9
5 MEM_MA_DATA10 >> 37 DQ10
5 MEM_MA_DATA11 >> 20 DQ11
5 MEM_MA_DATA12 >> 22 DQ12
5 MEM_MA_DATA13 >> 38 DQ13
5 MEM_MA_DATA14 >> 43 DQ14
5 MEM_MA_DATA15 >> 45 DQ15
5 MEM_MA_DATA16 >> 55 DQ16
5 MEM_MA_DATA17 >> 57 DQ17
5 MEM_MA_DATA18 >> 44 DQ18
5 MEM_MA_DATA19 >> 46 DQ19
5 MEM_MA_DATA20 >> 58 DQ20
5 MEM_MA_DATA21 >> 61 DQ21
5 MEM_MA_DATA22 >> 76 DQ22
5 MEM_MA_DATA23 >> 77 DQ23
5 MEM_MA_DATA24 >> 62 DQ24
5 MEM_MA_DATA25 >> 64 DQ25
5 MEM_MA_DATA26 >> 74 DQ26
5 MEM_MA_DATA27 >> 75 DQ27
5 MEM_MA_DATA28 >> 62 DQ28
5 MEM_MA_DATA29 >> 64 DQ29
5 MEM_MA_DATA30 >> 76 DQ30
5 MEM_MA_DATA31 >> 123 DQ31
5 MEM_MA_DATA32 >> 125 DQ32
5 MEM_MA_DATA33 >> 135 DQ33
5 MEM_MA_DATA34 >> 137 DQ34
5 MEM_MA_DATA35 >> 124 DQ35
5 MEM_MA_DATA36 >> 126 DQ36
5 MEM_MA_DATA37 >> 134 DQ37
5 MEM_MA_DATA38 >> 136 DQ38
5 MEM_MA_DATA39 >> 141 DQ39
5 MEM_MA_DATA40 >> 143 DQ40
5 MEM_MA_DATA41 >> 144 DQ41
5 MEM_MA_DATA42 >> 151 DQ42
5 MEM_MA_DATA43 >> 153 DQ43
5 MEM_MA_DATA44 >> 140 DQ44
5 MEM_MA_DATA45 >> 142 DQ45
5 MEM_MA_DATA46 >> 152 DQ46
5 MEM_MA_DATA47 >> 154 DQ47
5 MEM_MA_DATA48 >> 157 DQ48
5 MEM_MA_DATA49 >> 159 DQ49
5 MEM_MA_DATA50 >> 173 DQ50
5 MEM_MA_DATA51 >> 175 DQ51
5 MEM_MA_DATA52 >> 158 DQ52
5 MEM_MA_DATA53 >> 160 DQ53
5 MEM_MA_DATA54 >> 174 DQ54
5 MEM_MA_DATA55 >> 176 DQ55
5 MEM_MA_DATA56 >> 179 DQ56
5 MEM_MA_DATA57 >> 181 DQ57
5 MEM_MA_DATA58 >> 189 DQ58
5 MEM_MA_DATA59 >> 191 DQ59
5 MEM_MA_DATA60 >> 180 DQ60
5 MEM_MA_DATA61 >> 182 DQ61
5 MEM_MA_DATA62 >> 192 DQ62
5 MEM_MA_DATA63 >> 194 DQ63

5 MEM_MA_DQS0_N >> 11 DQS0#
5 MEM_MA_DQS1_N >> 29 DQS1#
5 MEM_MA_DQS2_N >> 49 DQS2#
5 MEM_MA_DQS3_N >> 68 DQS3#
5 MEM_MA_DQS4_N >> 122 DQS4#
5 MEM_MA_DQS5_N >> 146 DQS5#
5 MEM_MA_DQS6_N >> 167 DQS6#
5 MEM_MA_DQS7_N >> 186 DQS7#

5 MEM_MA_DQS0_P >> 13 DQS0#
5 MEM_MA_DQS1_P >> 31 DQS1#
5 MEM_MA_DQS2_P >> 51 DQS2#
5 MEM_MA_DQS3_P >> 70 DQS3#
5 MEM_MA_DQS4_P >> 131 DQS4#
5 MEM_MA_DQS5_P >> 148 DQS5#
5 MEM_MA_DQS6_P >> 169 DQS6#
5 MEM_MA_DQS7_P >> 188 DQS7#

5,18 MEM_MA0_ODT0 >> 114 OTD0
5,18 MEM_MA0_ODT1 >> 119 OTD1



Place C2.2uF and 0.1uF < 500mils from DDR connector

ADIMM2

A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
A14
A15
A16/BA2

BA0
BA1

DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
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DQ35
DQ36
DQ37
DQ38
DQ39
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63

DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
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DQ21
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DQ63

DQS0#
DQS1#
DQS2#
DQS3#
DQS4#
DQS5#
DQS6#
DQS7#

DQS0#
DQS1#
DQS2#
DQS3#
DQS4#
DQS5#
DQS6#
DQS7#

OTD0
OTD1

VREF
VSS
GND
MH1
MH2

SKT-SODIMM20020U4GP
62.10017.661

2ND = 62.10017.A41

NORMAL TYPE

RAS# >> 108 MEM_MA_RAS# 5,18
WE# >> 109 MEM_MA_WE# 5,18
CAS# >> 113 MEM_MA_CAS# 5,18
CS0# >> 110 MEM_MA0_CS#0 5,18
CS1# >> 115 MEM_MA0_CS#1 5,18
CKE0 >> 79 MEM_MA_CKE0 5,18
CKE1 >> 80 MEM_MA_CKE1 5,18
CK0 >> 30 MEM_MA_CLK0_P 5
CK0# >> 32 MEM_MA_CLK0_N 5
CK1 >> 164 MEM_MA_CLK1_P 5
CK1# >> 166 MEM_MA_CLK1_N 5
DM0 >> 10 MEM_MA_DM0 5
DM1 >> 26 MEM_MA_DM1 5
DM2 >> 52 MEM_MA_DM2 5
DM3 >> 67 MEM_MA_DM3 5
DM4 >> 130 MEM_MA_DM4 5
DM5 >> 147 MEM_MA_DM5 5
DM6 >> 170 MEM_MA_DM6 5
DM7 >> 185 MEM_MA_DM7 5

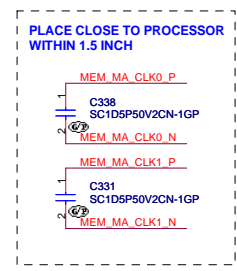
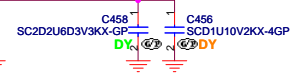
SDA >> 195 SMBD0_SB 3,12,17
SCL >> 197 SMBC0_SB 3,12,17
VDDSPD >> 199
SA0 >> 198
SA1 >> 200
NC#50 >> 50
NC#69 >> 69
NC#83 >> 83
NC#120 >> 120
NC#163/TEST >> 163
1D8V_S3 >> 81

VDD >> 81
VDD >> 82
VDD >> 87
VDD >> 88
VDD >> 96
VDD >> 103
VDD >> 104
VDD >> 111
VDD >> 112
VDD >> 117
VDD >> 118

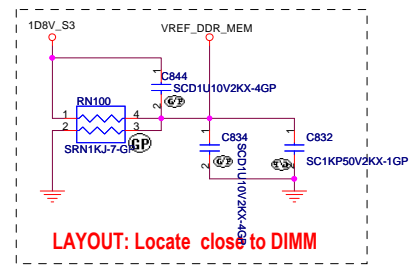
VSS >> 3
VSS >> 8
VSS >> 9
VSS >> 12
VSS >> 15
VSS >> 18
VSS >> 21
VSS >> 24
VSS >> 27
VSS >> 28
VSS >> 33
VSS >> 34
VSS >> 39
VSS >> 40
VSS >> 41
VSS >> 42
VSS >> 47
VSS >> 48
VSS >> 53
VSS >> 54
VSS >> 59
VSS >> 60
VSS >> 65
VSS >> 66
VSS >> 71
VSS >> 72
VSS >> 77
VSS >> 78
VSS >> 121
VSS >> 122
VSS >> 127
VSS >> 128
VSS >> 132
VSS >> 133
VSS >> 138
VSS >> 139
VSS >> 144
VSS >> 145
VSS >> 149
VSS >> 150
VSS >> 155
VSS >> 156
VSS >> 161
VSS >> 162
VSS >> 165
VSS >> 168
VSS >> 171
VSS >> 172
VSS >> 177
VSS >> 178
VSS >> 183
VSS >> 184
VSS >> 187
VSS >> 190
VSS >> 193
VSS >> 196
VSS >> 201
VSS >> 202

VSS >> 3
VSS >> 8
VSS >> 9
VSS >> 12
VSS >> 15
VSS >> 18
VSS >> 21
VSS >> 24
VSS >> 27
VSS >> 28
VSS >> 33
VSS >> 34
VSS >> 39
VSS >> 40
VSS >> 41
VSS >> 42
VSS >> 47
VSS >> 48
VSS >> 53
VSS >> 54
VSS >> 59
VSS >> 60
VSS >> 65
VSS >> 66
VSS >> 71
VSS >> 72
VSS >> 77
VSS >> 78
VSS >> 121
VSS >> 122
VSS >> 127
VSS >> 128
VSS >> 132
VSS >> 133
VSS >> 138
VSS >> 139
VSS >> 144
VSS >> 145
VSS >> 149
VSS >> 150
VSS >> 155
VSS >> 156
VSS >> 161
VSS >> 162
VSS >> 165
VSS >> 168
VSS >> 171
VSS >> 172
VSS >> 177
VSS >> 178
VSS >> 183
VSS >> 184
VSS >> 187
VSS >> 190
VSS >> 193
VSS >> 196
VSS >> 201
VSS >> 202

GND
MH1
MH2



DDR_VREF



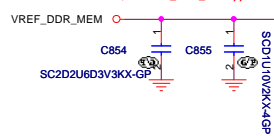
LAYOUT: Locate close to DIMM

5,18 MEM_MB_ADD0 >>> 102 A0
5,18 MEM_MB_ADD1 >>> 101 A1
5,18 MEM_MB_ADD2 >>> 100 A2
5,18 MEM_MB_ADD3 >>> 99 A3
5,18 MEM_MB_ADD4 >>> 98 A4
5,18 MEM_MB_ADD5 >>> 97 A5
5,18 MEM_MB_ADD6 >>> 96 A6
5,18 MEM_MB_ADD7 >>> 95 A7
5,18 MEM_MB_ADD8 >>> 94 A8
5,18 MEM_MB_ADD9 >>> 93 A9
5,18 MEM_MB_ADD10 >>> 105 A10/AP
5,18 MEM_MB_ADD11 >>> 90 A11
5,18 MEM_MB_ADD12 >>> 116 A12
5,18 MEM_MB_ADD13 >>> 89 A13
5,18 MEM_MB_ADD14 >>> 88 A14
5,18 MEM_MB_ADD15 >>> 84 A15
5,18 MEM_MB_BANK2 >>> 107 BA0
5,18 MEM_MB_BANK0 >>> 106 BA1
5,18 MEM_MB_BANK1 >>> 106 BA1

5 MEM_MB_DATA0 >>> 5 D00
5 MEM_MB_DATA1 >>> 7 D01
5 MEM_MB_DATA2 >>> 17 D02
5 MEM_MB_DATA3 >>> 19 D03
5 MEM_MB_DATA4 >>> 4 D04
5 MEM_MB_DATA5 >>> 6 D05
5 MEM_MB_DATA6 >>> 14 D06
5 MEM_MB_DATA7 >>> 16 D07
5 MEM_MB_DATA8 >>> 23 D08
5 MEM_MB_DATA9 >>> 25 D09
5 MEM_MB_DATA10 >>> 35 D10
5 MEM_MB_DATA11 >>> 37 D11
5 MEM_MB_DATA12 >>> 20 D12
5 MEM_MB_DATA13 >>> 22 D13
5 MEM_MB_DATA14 >>> 36 D14
5 MEM_MB_DATA15 >>> 38 D15
5 MEM_MB_DATA16 >>> 43 D16
5 MEM_MB_DATA17 >>> 45 D17
5 MEM_MB_DATA18 >>> 55 D18
5 MEM_MB_DATA19 >>> 57 D19
5 MEM_MB_DATA20 >>> 44 D20
5 MEM_MB_DATA21 >>> 46 D21
5 MEM_MB_DATA22 >>> 58 D22
5 MEM_MB_DATA23 >>> 61 D23
5 MEM_MB_DATA24 >>> 58 D24
5 MEM_MB_DATA25 >>> 63 D25
5 MEM_MB_DATA26 >>> 73 D26
5 MEM_MB_DATA27 >>> 75 D27
5 MEM_MB_DATA28 >>> 62 D28
5 MEM_MB_DATA29 >>> 64 D29
5 MEM_MB_DATA30 >>> 74 D30
5 MEM_MB_DATA31 >>> 76 D31
5 MEM_MB_DATA32 >>> 123 D32
5 MEM_MB_DATA33 >>> 125 D33
5 MEM_MB_DATA34 >>> 135 D34
5 MEM_MB_DATA35 >>> 137 D35
5 MEM_MB_DATA36 >>> 124 D36
5 MEM_MB_DATA37 >>> 126 D37
5 MEM_MB_DATA38 >>> 134 D38
5 MEM_MB_DATA39 >>> 136 D39
5 MEM_MB_DATA40 >>> 141 D40
5 MEM_MB_DATA41 >>> 143 D41
5 MEM_MB_DATA42 >>> 151 D42
5 MEM_MB_DATA43 >>> 153 D43
5 MEM_MB_DATA44 >>> 140 D44
5 MEM_MB_DATA45 >>> 142 D45
5 MEM_MB_DATA46 >>> 152 D46
5 MEM_MB_DATA47 >>> 154 D47
5 MEM_MB_DATA48 >>> 157 D48
5 MEM_MB_DATA49 >>> 159 D49
5 MEM_MB_DATA50 >>> 173 D50
5 MEM_MB_DATA51 >>> 175 D51
5 MEM_MB_DATA52 >>> 158 D52
5 MEM_MB_DATA53 >>> 160 D53
5 MEM_MB_DATA54 >>> 174 D54
5 MEM_MB_DATA55 >>> 176 D55
5 MEM_MB_DATA56 >>> 179 D56
5 MEM_MB_DATA57 >>> 181 D57
5 MEM_MB_DATA58 >>> 189 D58
5 MEM_MB_DATA59 >>> 191 D59
5 MEM_MB_DATA60 >>> 180 D60
5 MEM_MB_DATA61 >>> 182 D61
5 MEM_MB_DATA62 >>> 192 D62
5 MEM_MB_DATA63 >>> 194 D63

5 MEM_MB_DQS0_N >>> 110 DQS0#
5 MEM_MB_DQS1_N >>> 29 DQS1#
5 MEM_MB_DQS2_N >>> 49 DQS2#
5 MEM_MB_DQS3_N >>> 68 DQS3#
5 MEM_MB_DQS4_N >>> 129 DQS4#
5 MEM_MB_DQS5_N >>> 146 DQS5#
5 MEM_MB_DQS6_N >>> 167 DQS6#
5 MEM_MB_DQS7_N >>> 186 DQS7#
5 MEM_MB_DQS0_P >>> 13 DQS0#
5 MEM_MB_DQS1_P >>> 31 DQS1#
5 MEM_MB_DQS2_P >>> 51 DQS2#
5 MEM_MB_DQS3_P >>> 70 DQS3#
5 MEM_MB_DQS4_P >>> 131 DQS4#
5 MEM_MB_DQS5_P >>> 148 DQS5#
5 MEM_MB_DQS6_P >>> 169 DQS6#
5 MEM_MB_DQS7_P >>> 188 DQS7#

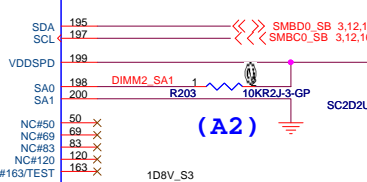
5,18 MEM_MB_ODT0 >>> 114 OTD0
5,18 MEM_MB_ODT1 >>> 119 OTD1



Place C2.2uF and 0.1uF < 500mils from DDR connector

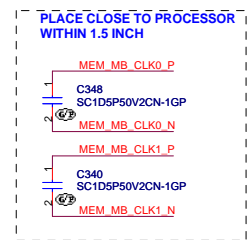
REVERSE TYPE

RAS# 108 A0
WE# 109 A1
CAS# 113 A2
CS0# 110 A3
CS1# 115 A4
CKE0 79 A5
CKE1 80 A6
CK0 30 A7
CK0# 32 A8
CK1 164 A9
CK1# 166 A10
DM0 10 A11
DM1 26 A12
DM2 52 A13
DM3 130 A14
DM4 147 A15
DM5 170 A16/BA2
DM6 185 A17
DM7 185 A18



NC#50 50 X
NC#69 69 X
NC#83 83 X
NC#120 120 X
NC#163/TEST 163 X

VDD 81
VDD 82
VDD 87
VDD 88
VDD 95
VDD 96
VDD 103
VDD 104
VDD 111
VDD 112
VDD 117
VDD 118
VSS 3
VSS 8
VSS 9
VSS 12
VSS 15
VSS 18
VSS 21
VSS 24
VSS 27
VSS 28
VSS 33
VSS 34
VSS 38
VSS 40
VSS 41
VSS 42
VSS 47
VSS 48
VSS 53
VSS 54
VSS 59
VSS 60
VSS 65
VSS 66
VSS 71
VSS 72
VSS 77
VSS 78
VSS 121
VSS 122
VSS 127
VSS 128
VSS 132
VSS 133
VSS 138
VSS 139
VSS 144
VSS 145
VSS 149
VSS 150
VSS 155
VSS 156
VSS 161
VSS 162
VSS 165
VSS 168
VSS 171
VSS 172
VSS 177
VSS 178
VSS 183
VSS 184
VSS 187
VSS 190
VSS 193
VSS 196
GND 201
MH2 GP



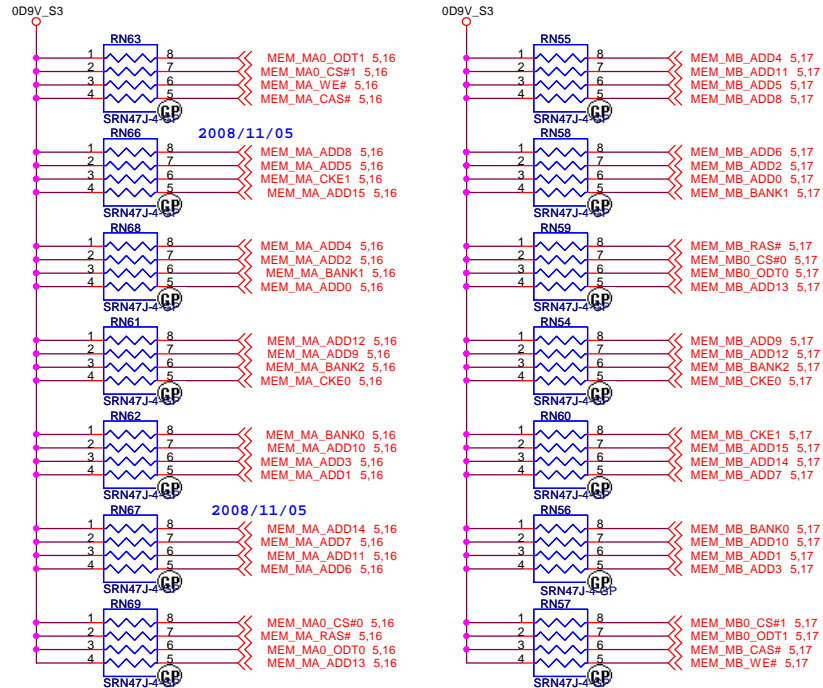
DDR2-200P-22-GP-U3
62.10017.A61
2ND = 62.10017.A51
Hl 9.2mm

<Core Design>

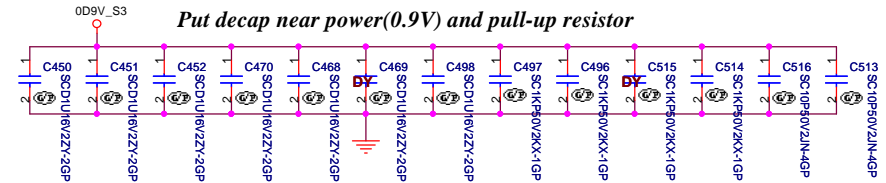
緯創資通 Wistron Corporation		
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Title		
DDR SO-DIMM SKT 2		
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PARALLEL TERMINATION

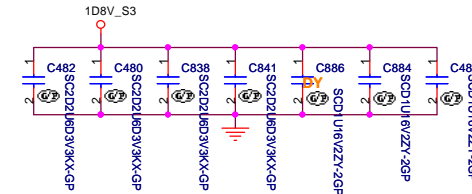
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

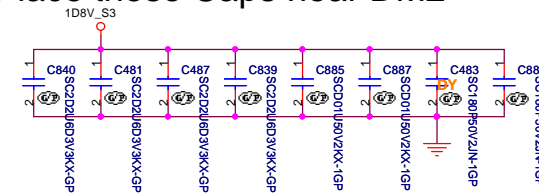


Place these Caps near DM1



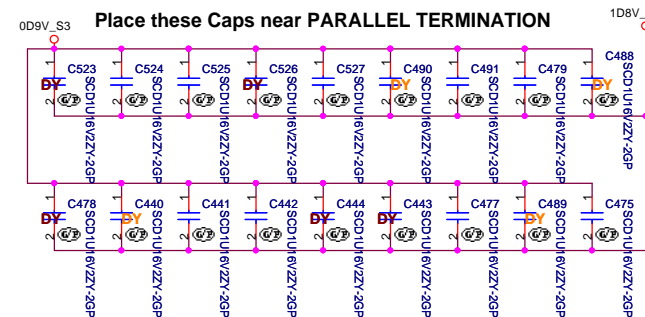
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0.9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0.9V_S3

Place these Caps near PARALLEL TERMINATION

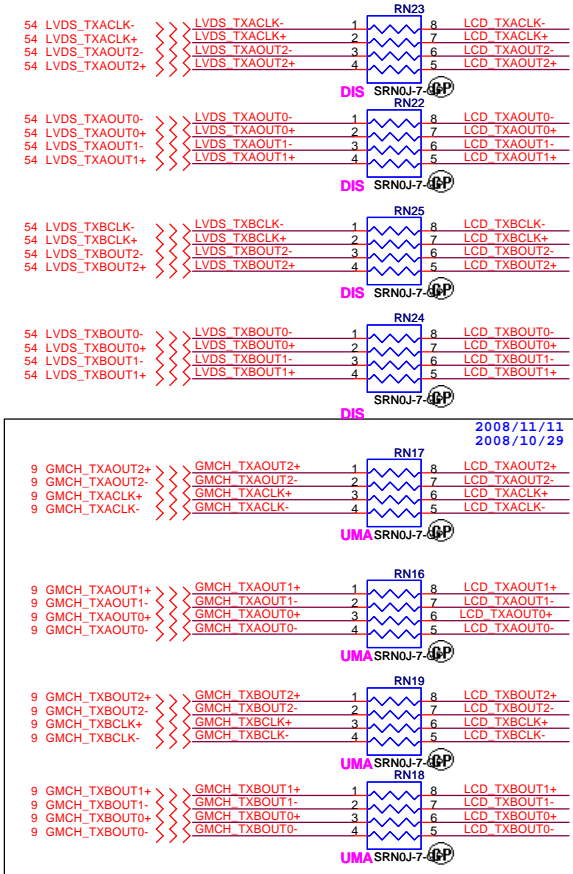
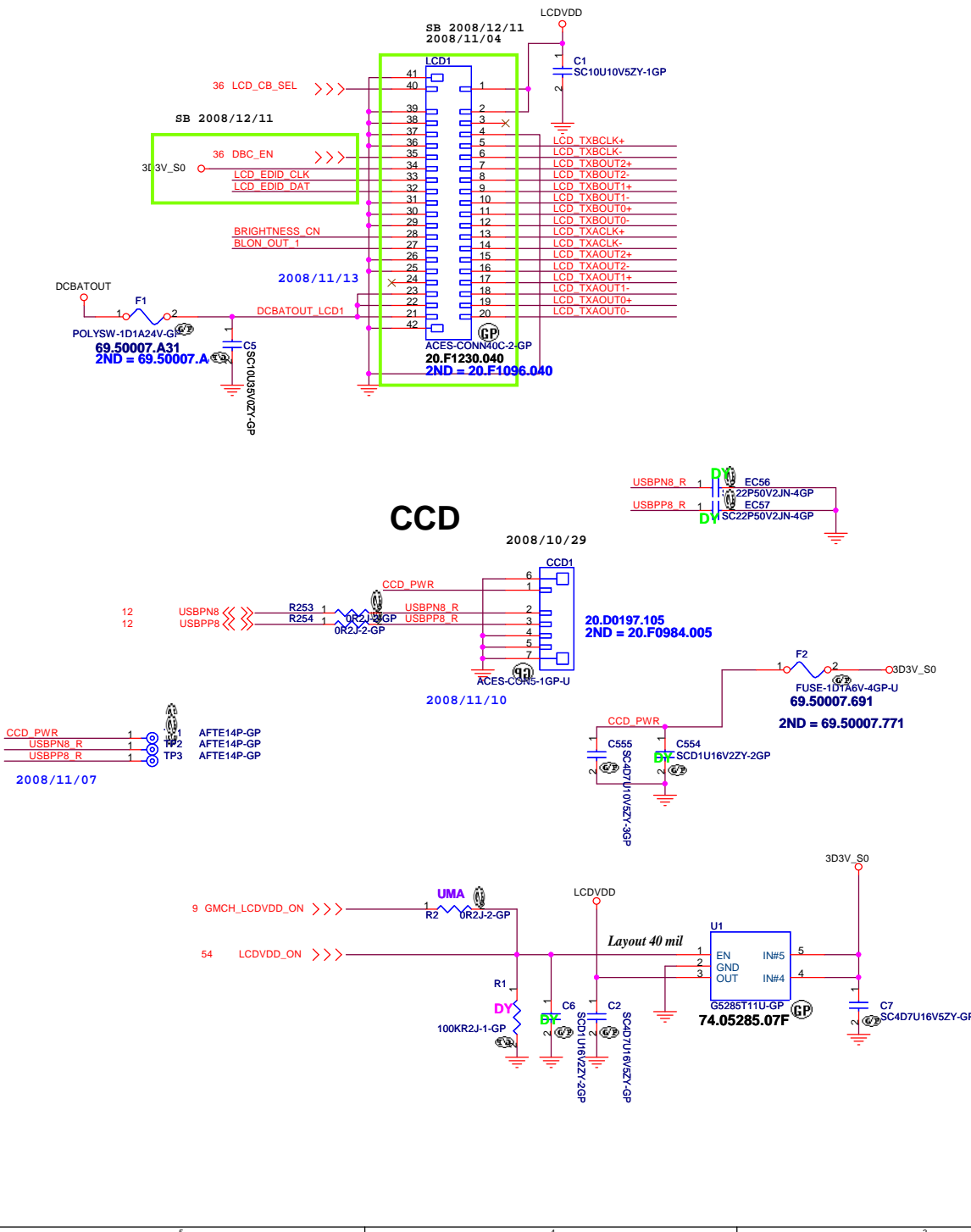


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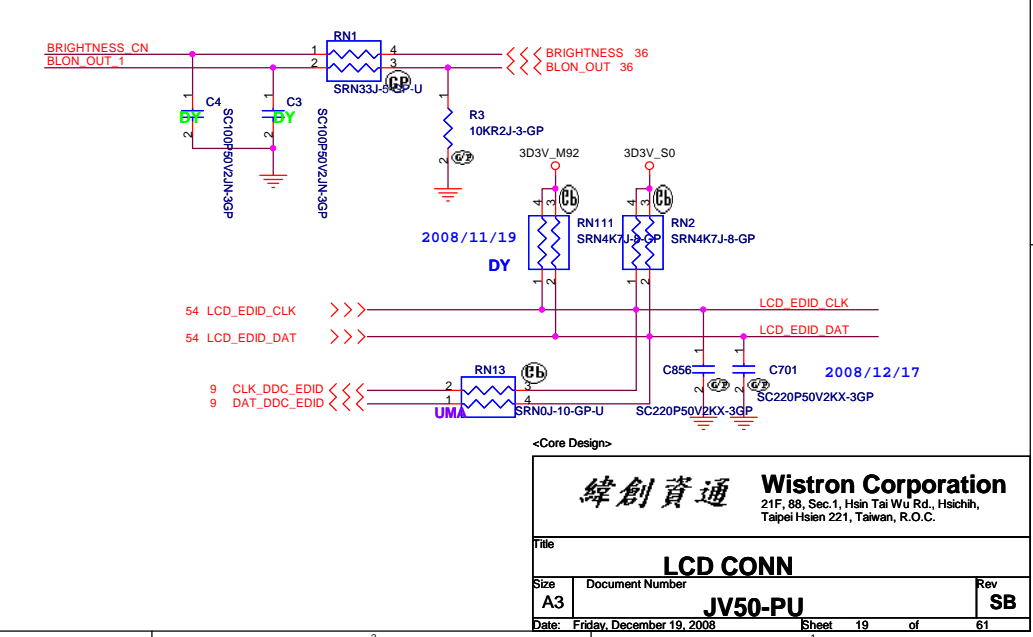
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DDR DAMPING & TERMINATION		
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LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

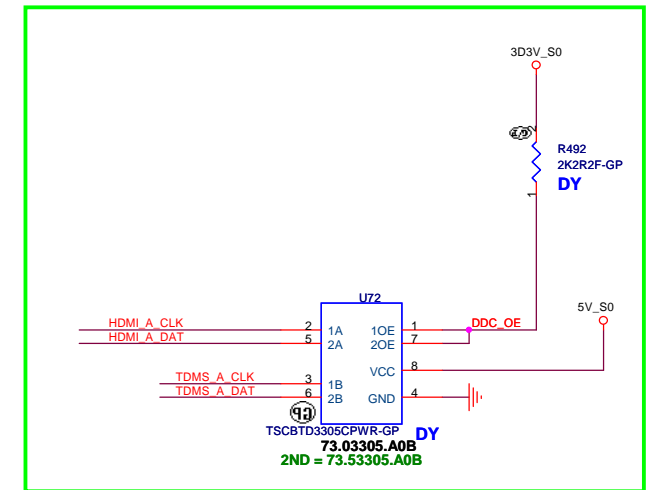
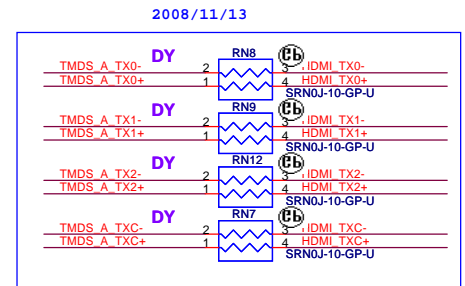
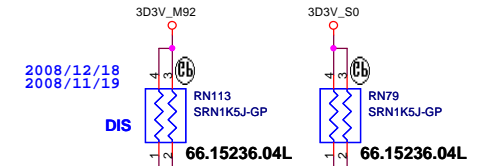


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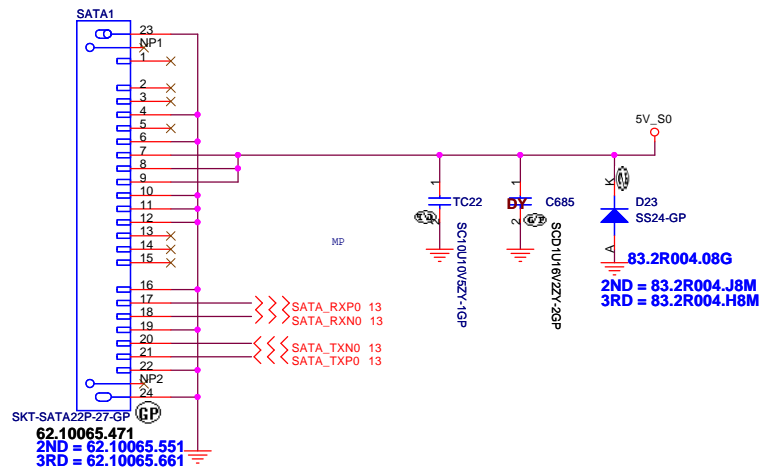
Wistron Corporation

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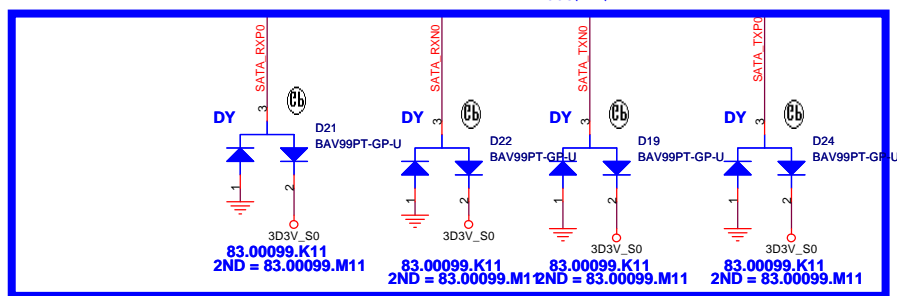
Title		
LCD CONN		
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SATA Connector



2008/12/17



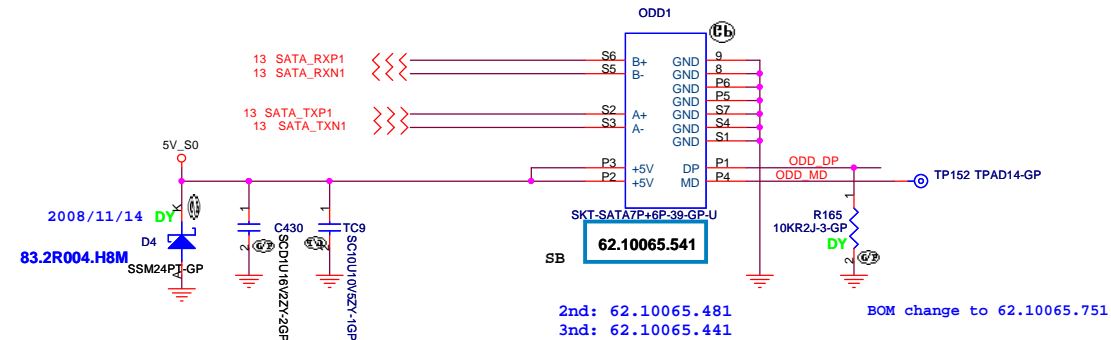
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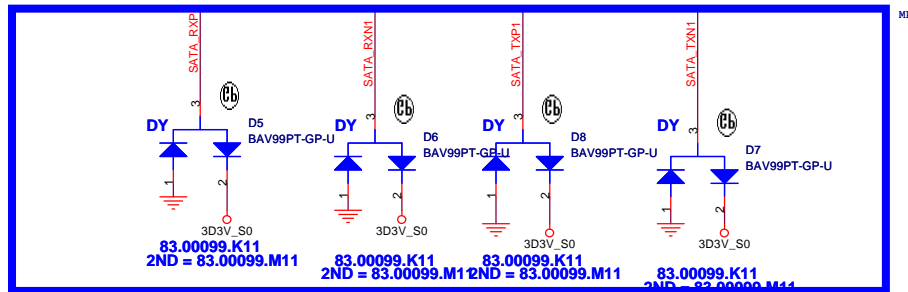
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SATA ODD Connector

2008/11/12



2008/12/17



<Core Design>

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Title

ODD

Size

Document Number

JV50-PU

Rev

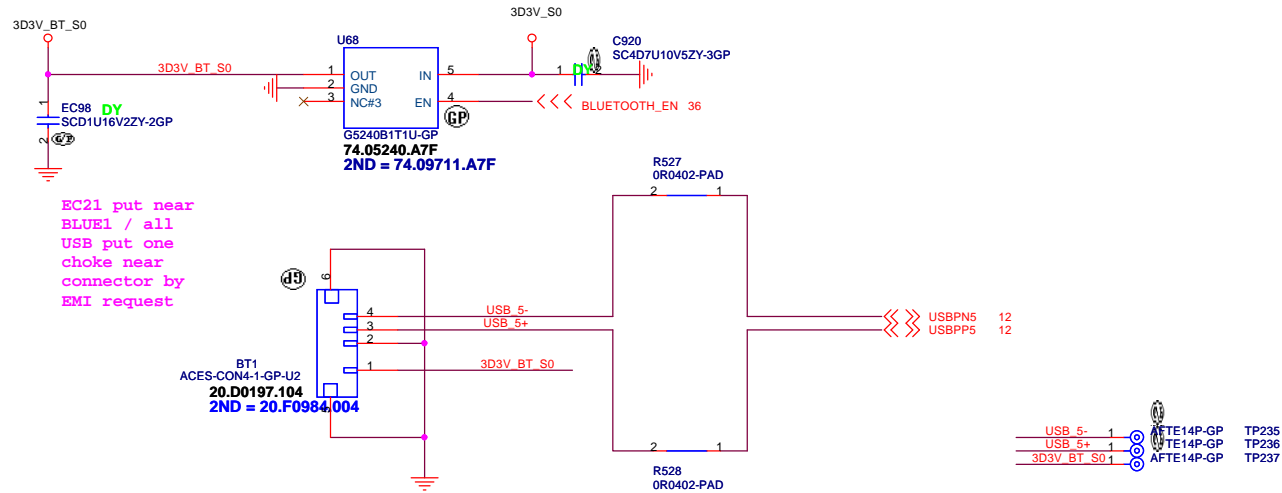
SB

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BLUETOOTH MODULE

1.5A / High Active Voltage 2V

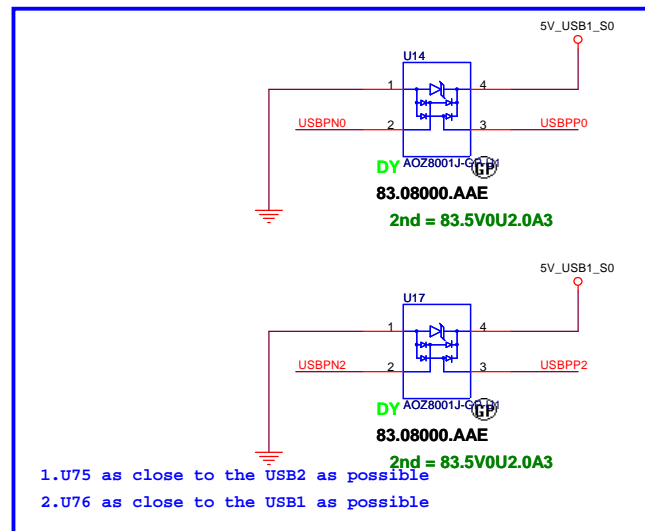
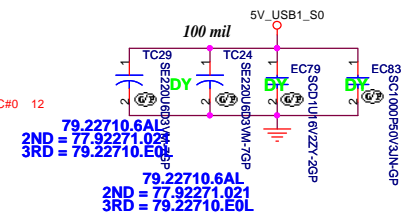
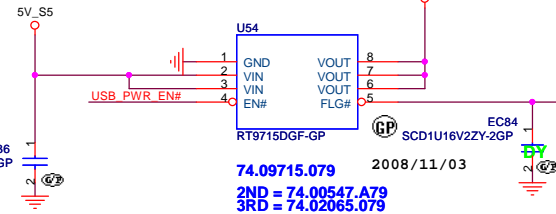
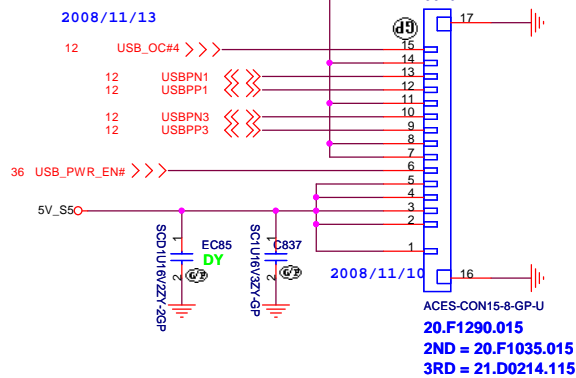
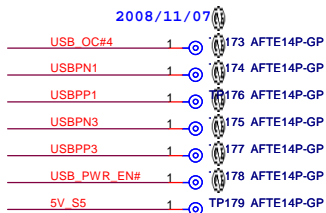
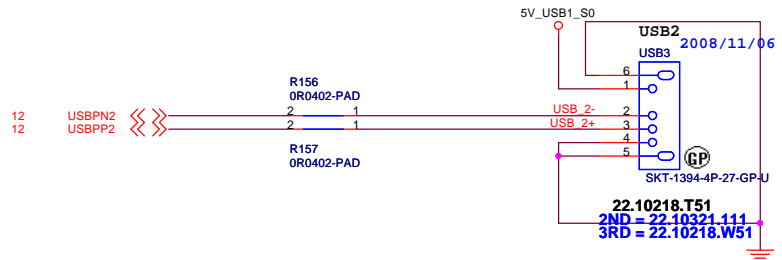
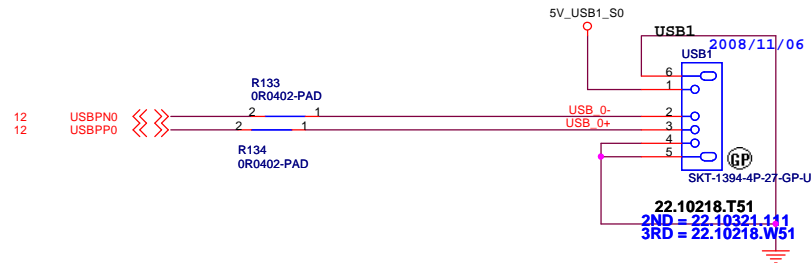


緯創資通

Wistron Corporation

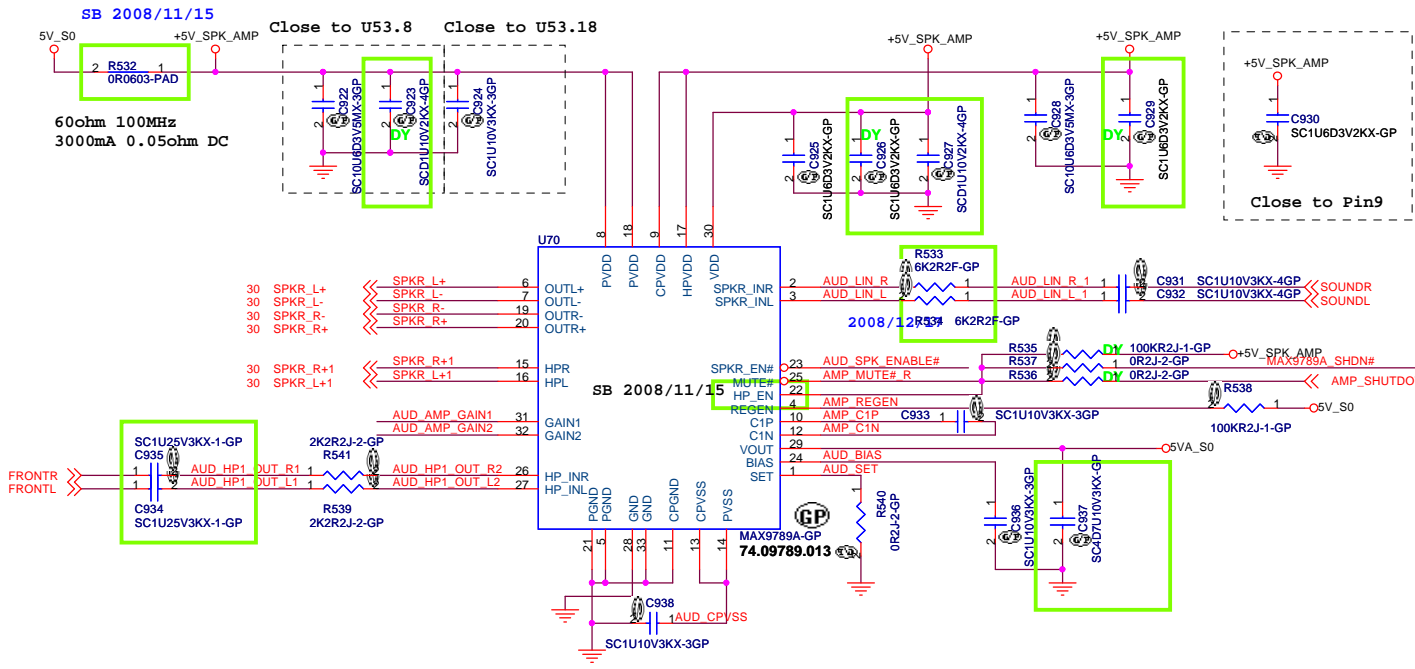
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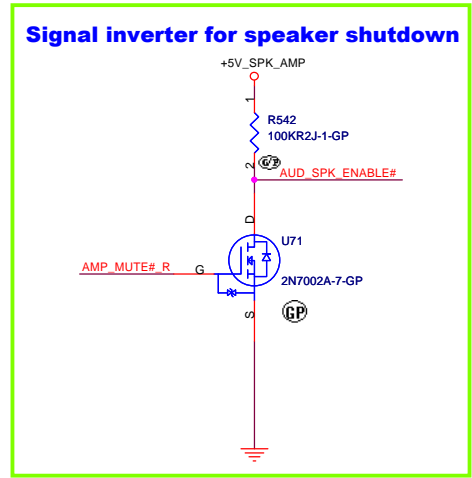
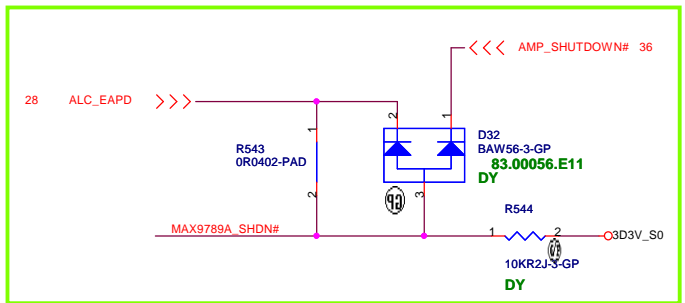
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

[illegible]



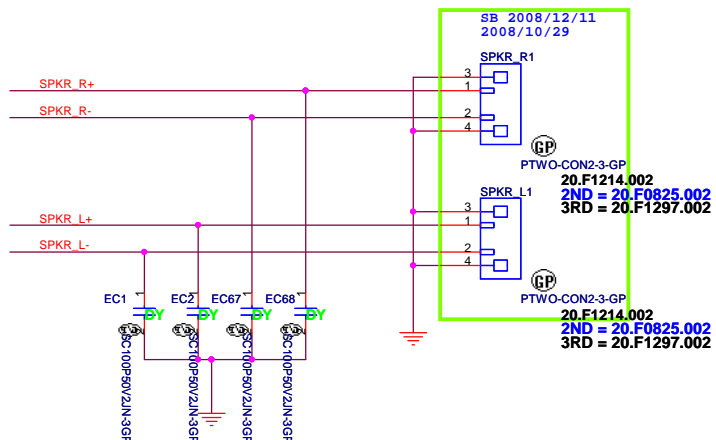
GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Internal Speaker

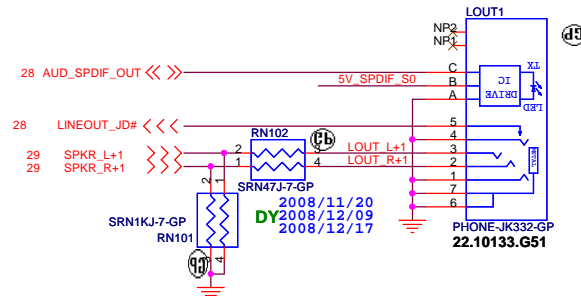
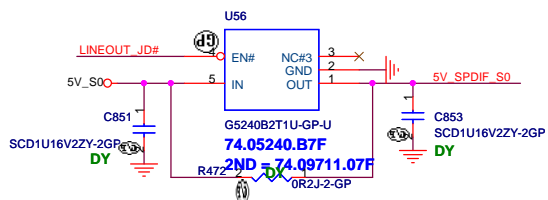
29 SPKR_L- <<<< SPKR_L-
29 SPKR_L+ <<<< SPKR_L+
29 SPKR_R- <<<< SPKR_R-
29 SPKR_R+ <<<< SPKR_R+



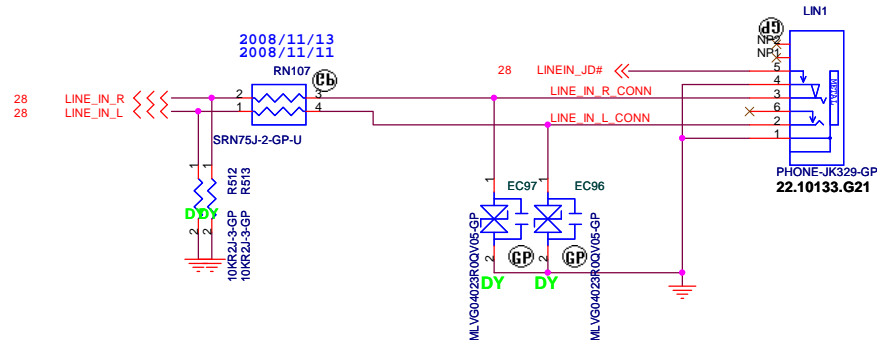
AUD_SPDIF_OUT 1 TE14P-GP TP164
5V_SPDIF_S0 1 TE14P-GP TP158
LINEOUT_JD# 1 TE14P-GP TP154
LOUT_R+1 1 TE14P-GP TP163
LOUT_L+1 1 TE14P-GP TP155
MIC_JD# 1 TE14P-GP TP168
AUD_MICIN_R_2 1 TE14P-GP TP166
AUD_MICIN_L_2 1 TE14P-GP TP165
INT_MIC_1 1 TE14P-GP TP4
LINEIN_JD# 1 TE14P-GP TP172
LINE_IN_R_CONN 1 TE14P-GP TP171
LINE_IN_L_CONN 1 AFTE14P-GP TP170

SPKR_L- 1 TE14P-GP TP5
SPKR_L+ 1 TE14P-GP TP6
SPKR_R- 1 TE14P-GP TP18
SPKR_R+ 1 AFTE14P-GP TP19

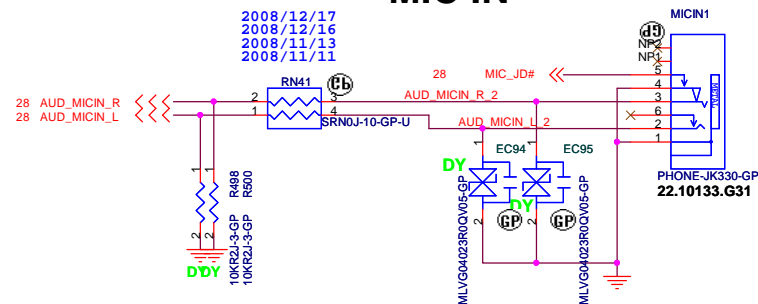
LINE OUT



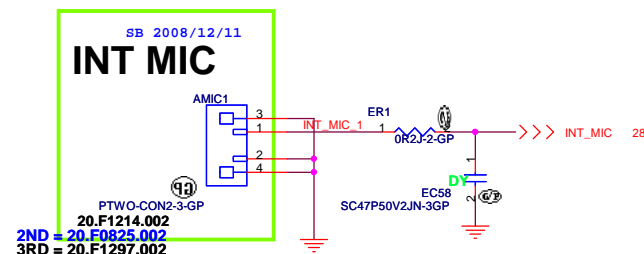
LINE IN



MIC IN



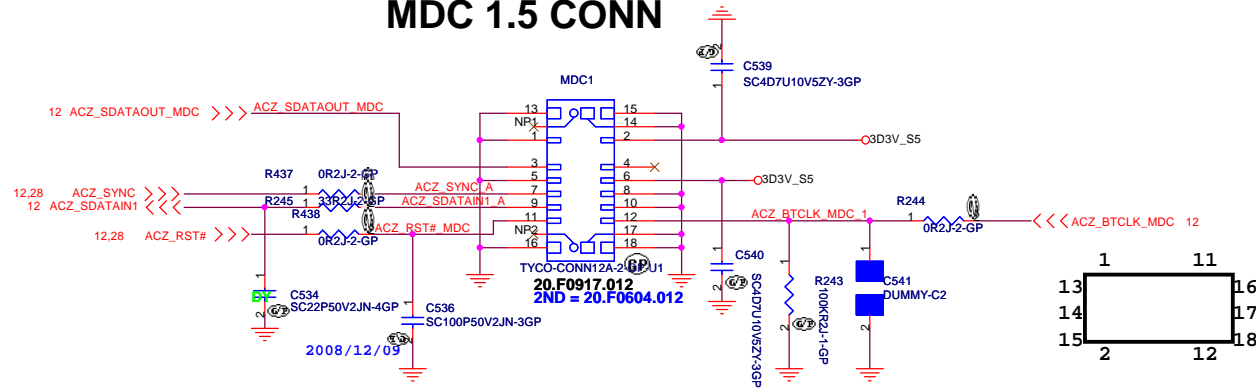
INT MIC



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AUDIO JACK			
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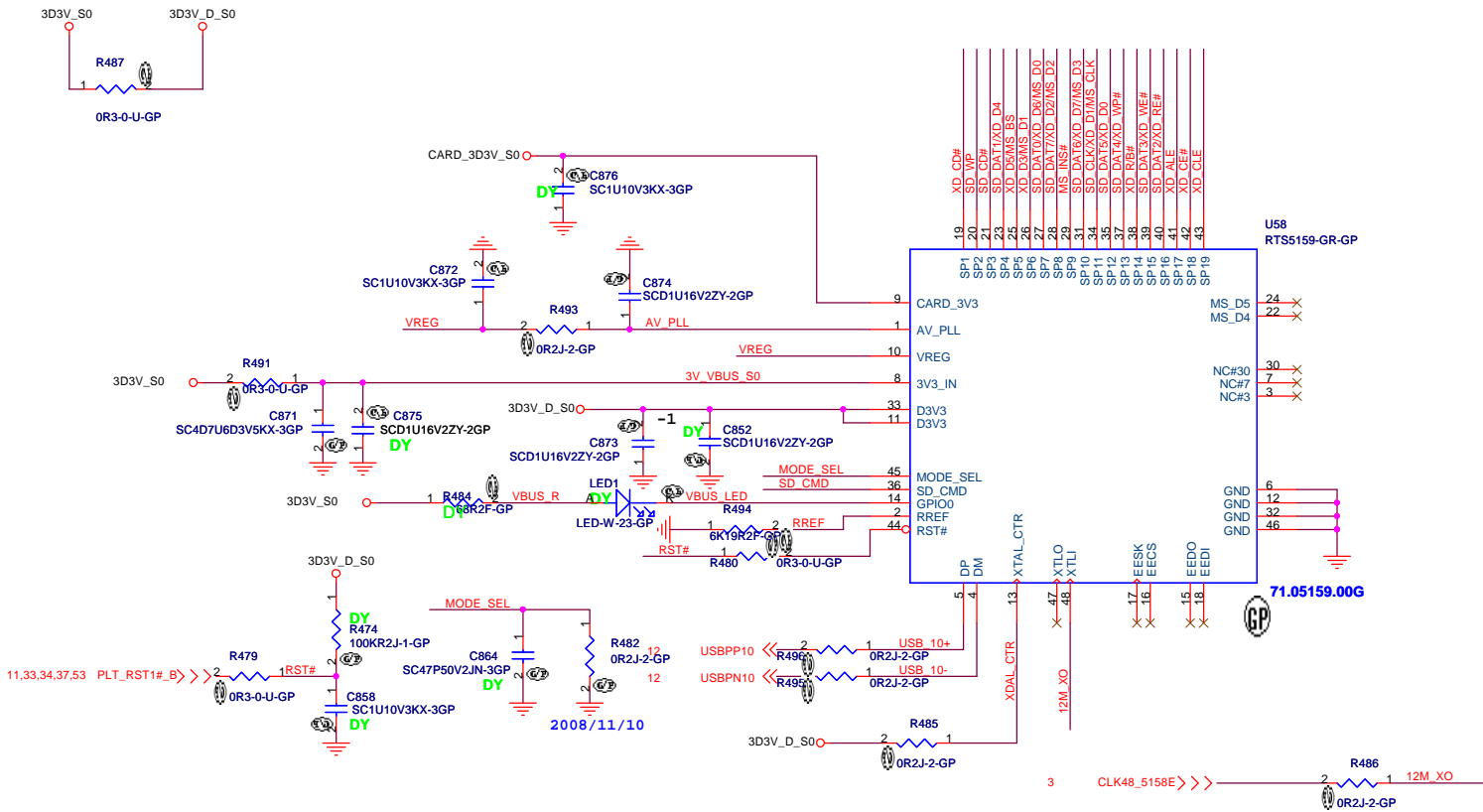
MDC 1.5 CONN



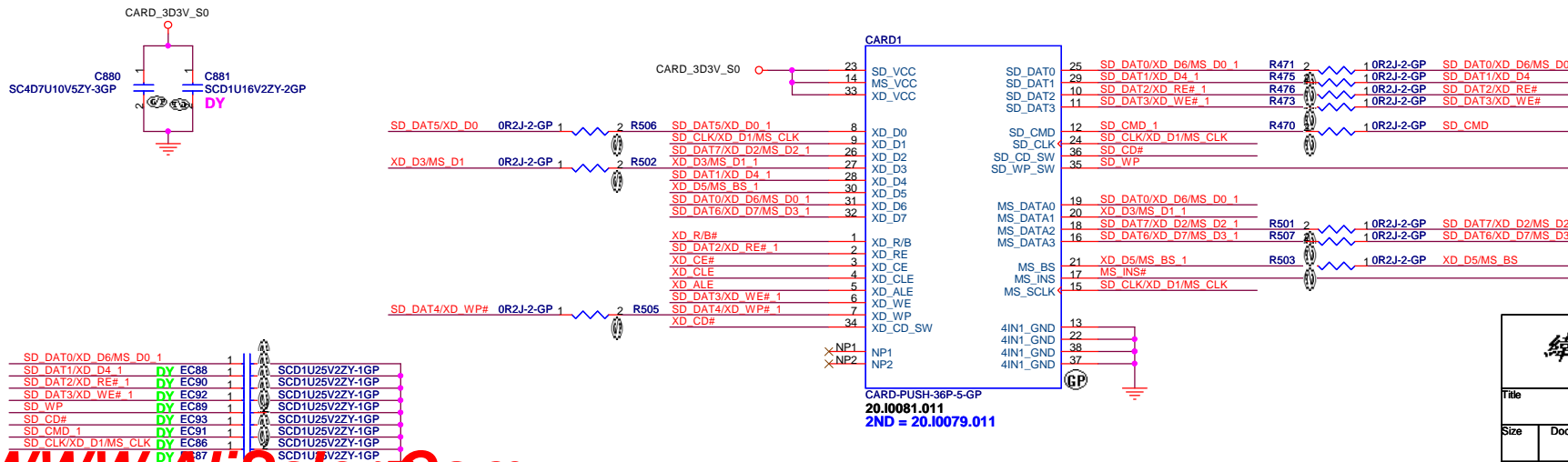
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title			MDC		
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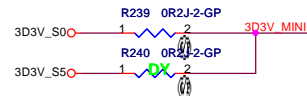
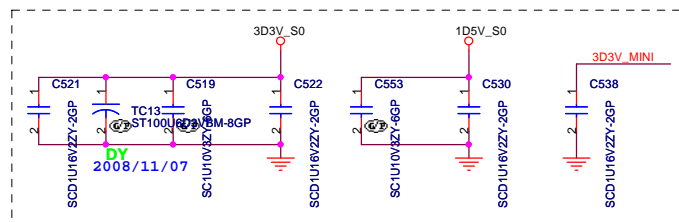
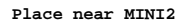
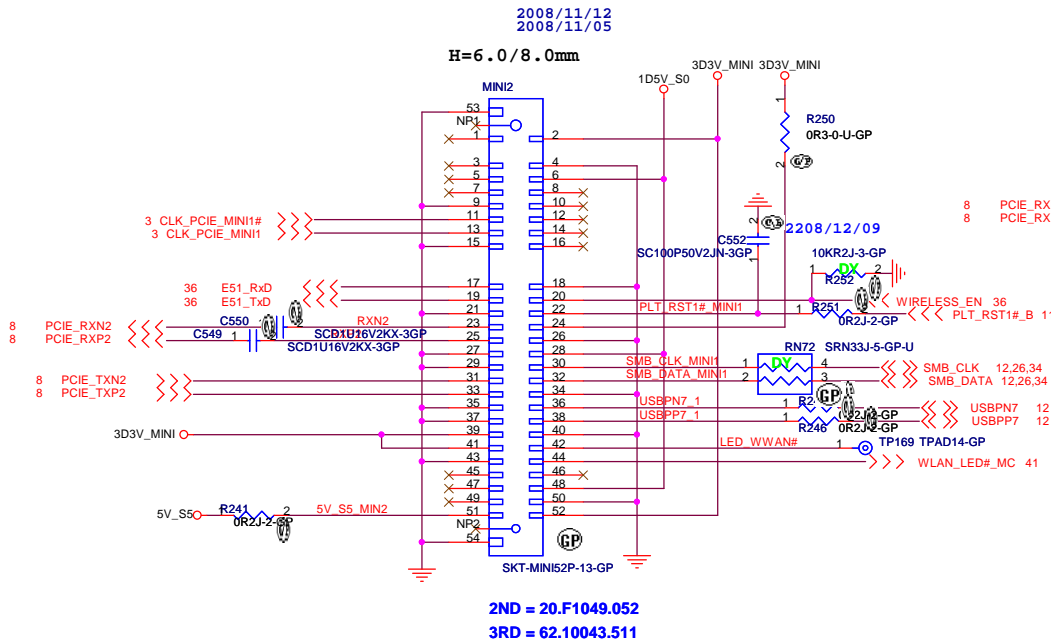


5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)

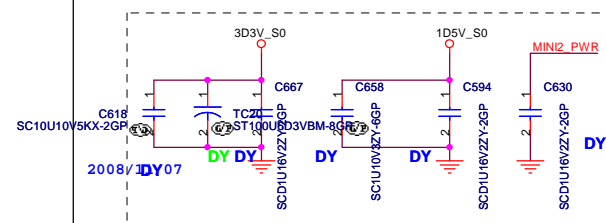
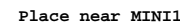
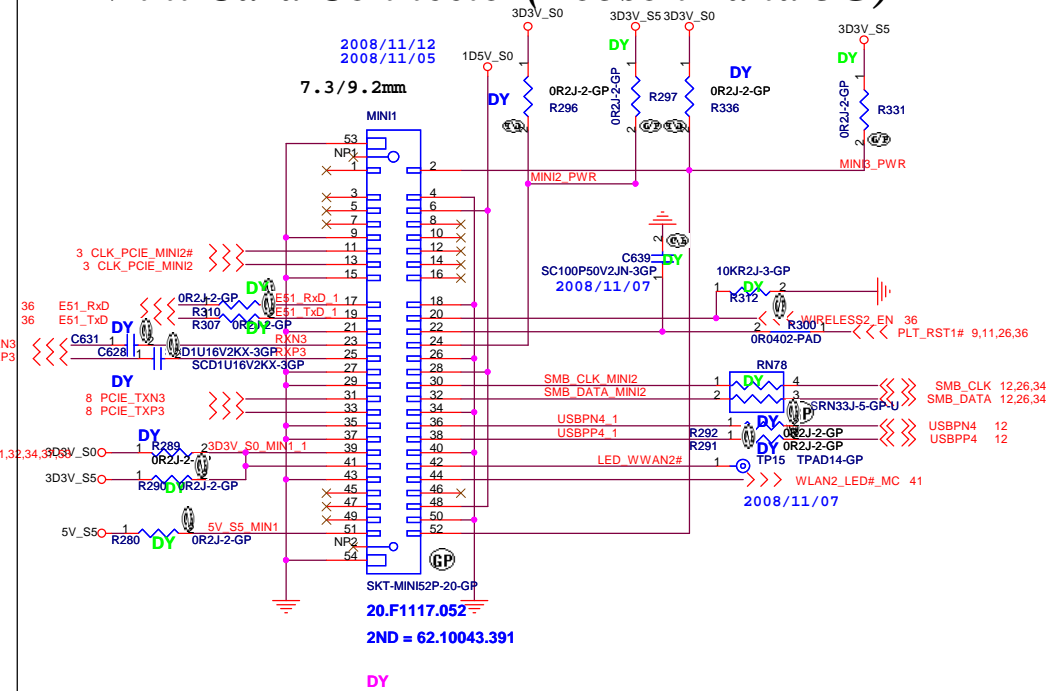


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CARDREADER- RTS5159	
Title Size Date: Friday, December 19, 2008	Document Number JV50-PU Sheet 32 of 61
Rev SB	

Mini Card Connector(WLAN)



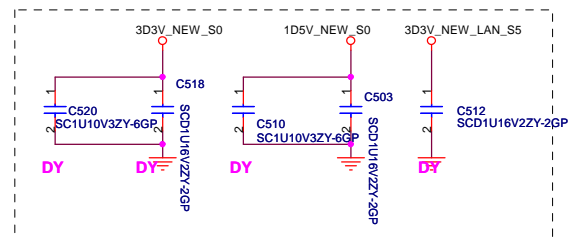
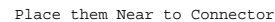
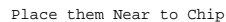
Mini Card Connector(Robson2 and 3G)



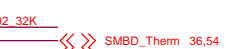
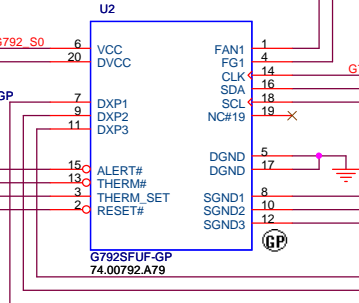
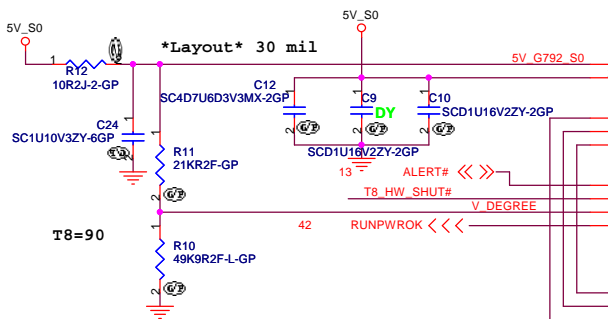
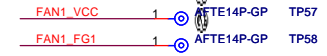
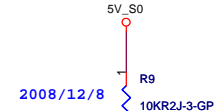
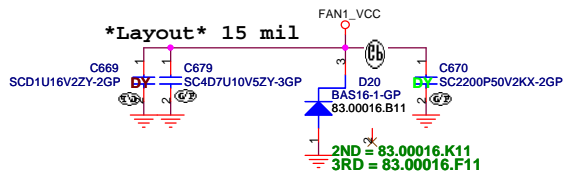
緯創資通 **Wistron Corporation**
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Title			
MINI CARD			
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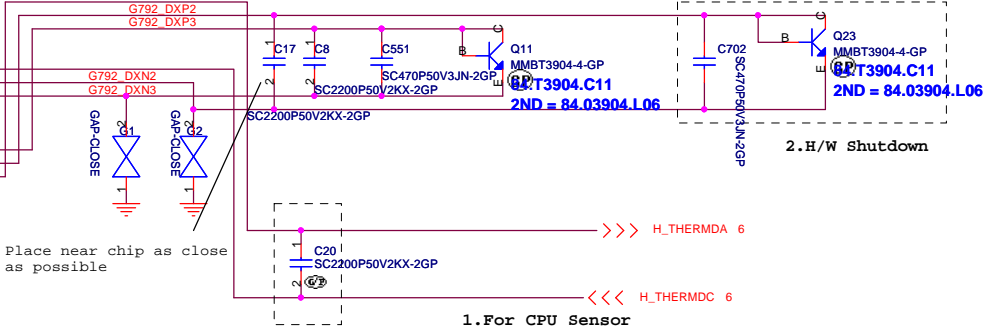
WWW.AliSaler.Com



Title			
NEW CARD			
Size	Document Number		Rev
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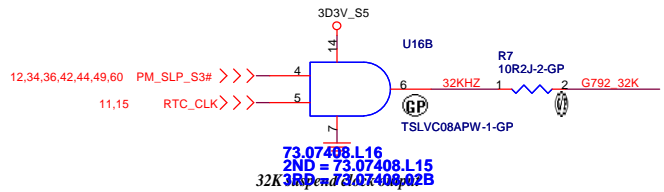


3.System Sensor, Put Plamrest.



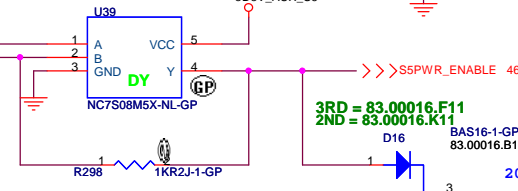
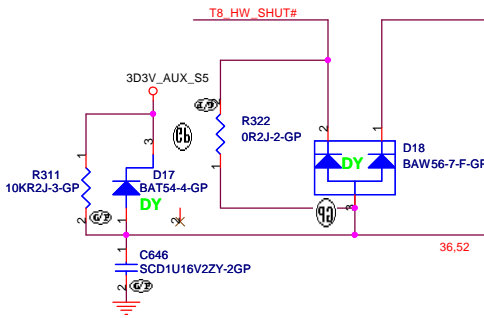
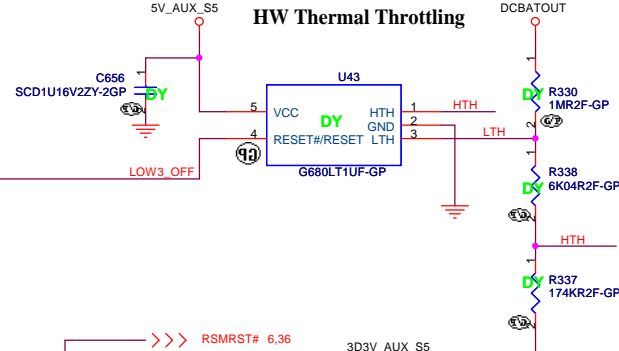
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

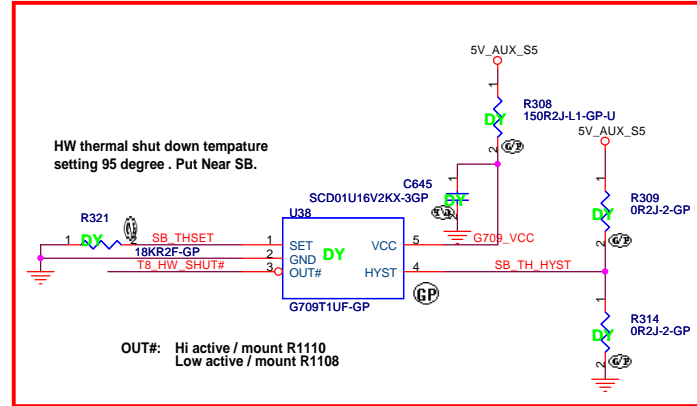


BL3#

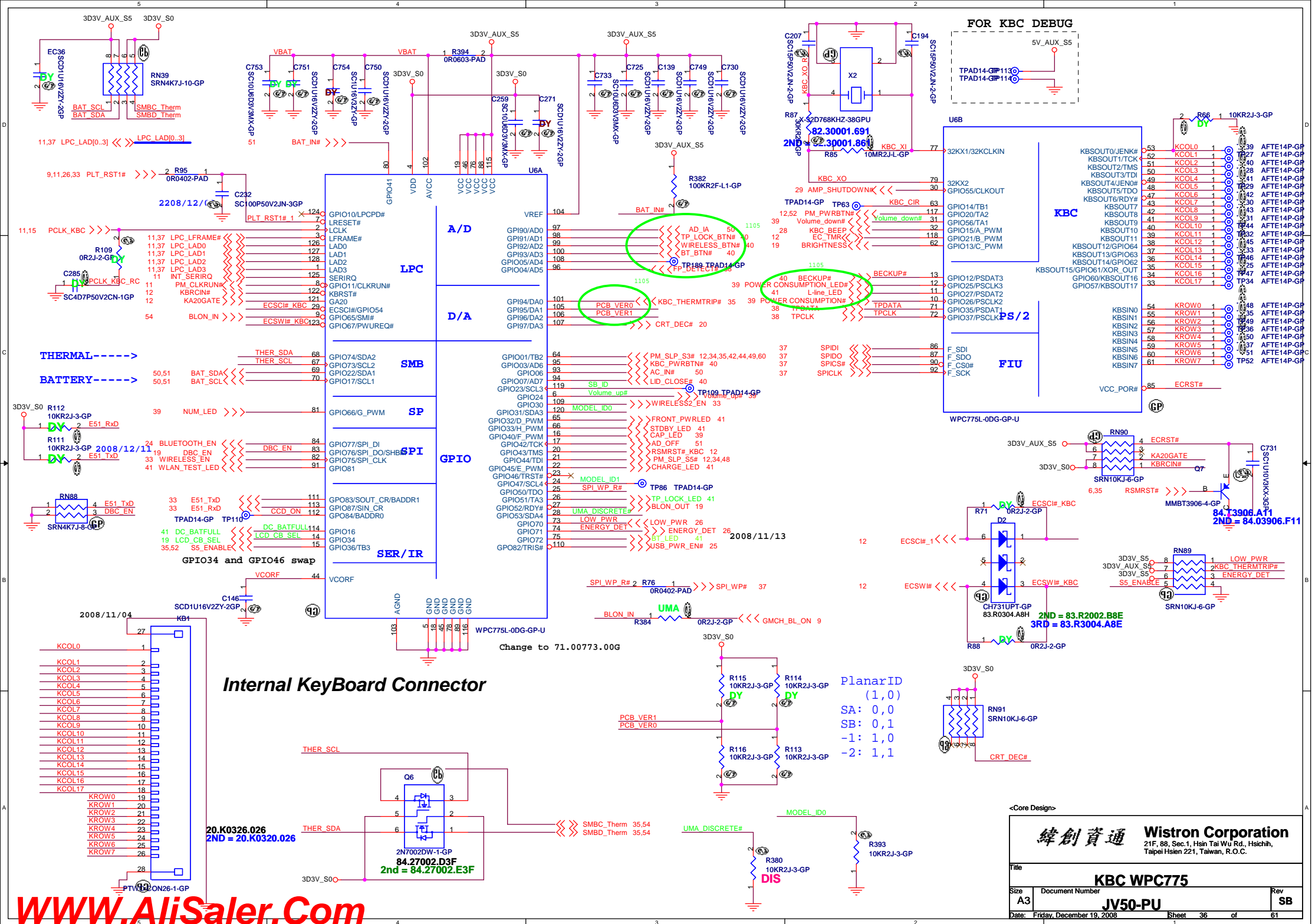
HW Thermal Throttling

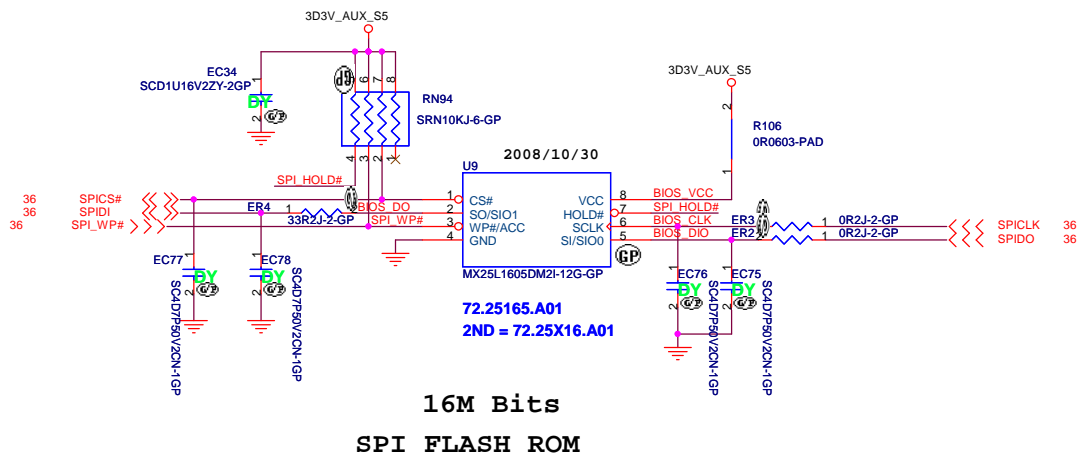


2008/11/07

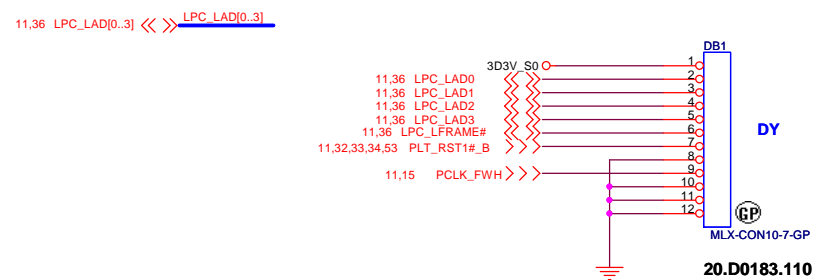


<Core Design>





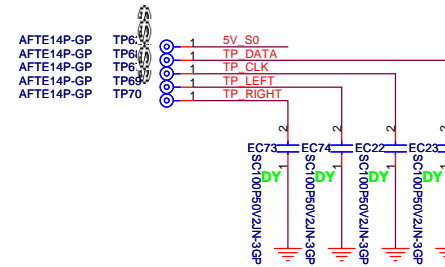
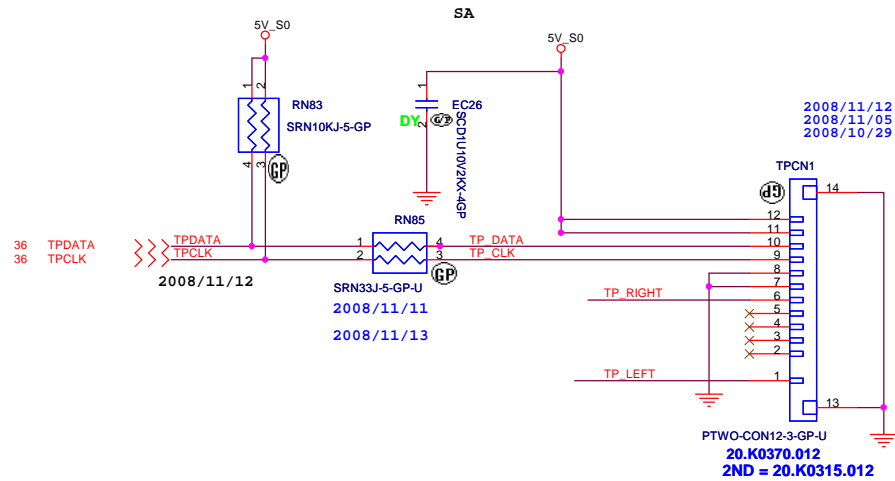
GOLDEN FINGER FOR DEBUG BOARD



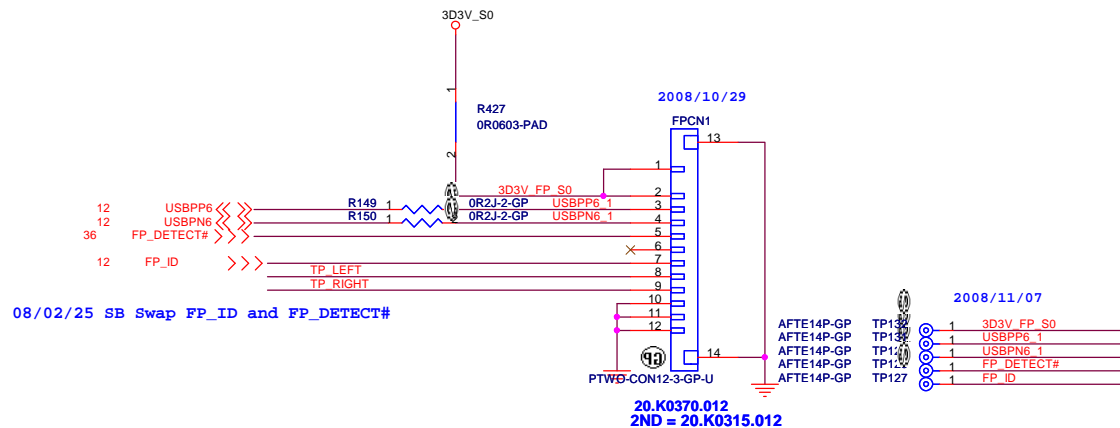
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BIOS			
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TOUCH PAD



Finger printer



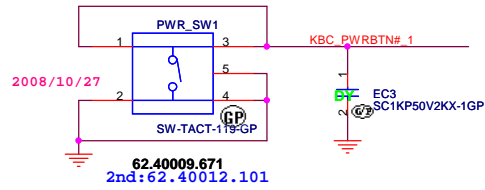
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Taipei Hsien 221, Taiwan, R.O.C.

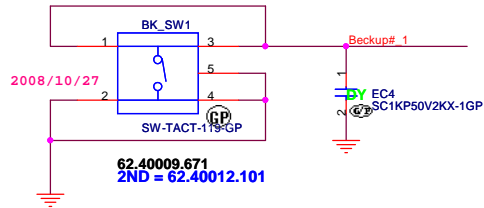
Title		Touch PAD/Finger printer	
Size	Document Number	Rev	
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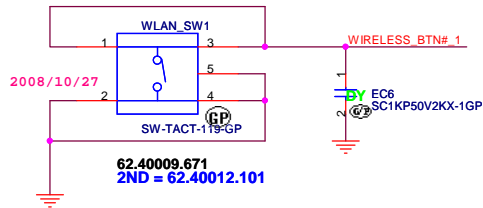
Power Button



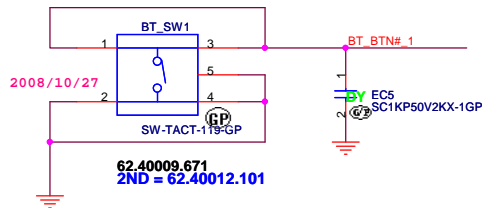
Beckup Button



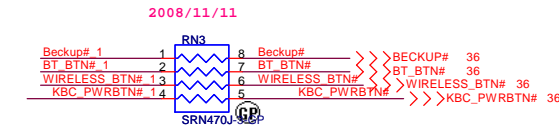
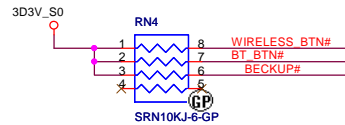
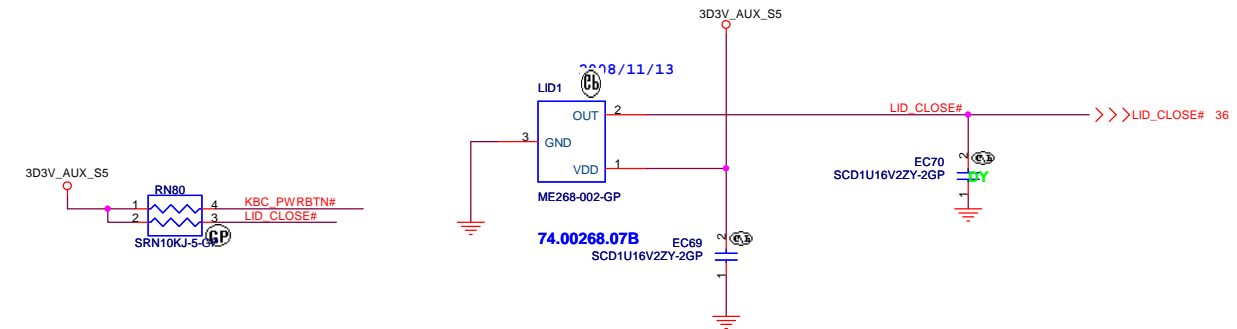
WIRELESS Button



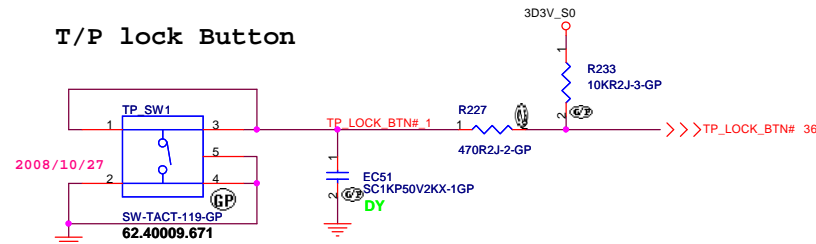
BT/3G Button



Cover Up Switch



T/P lock Button

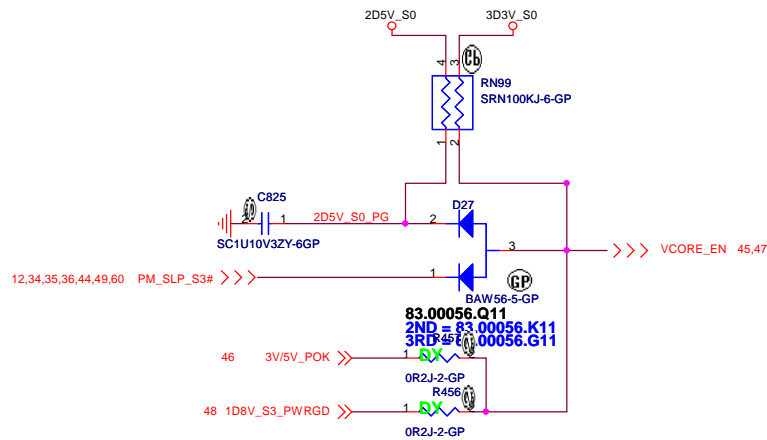


緯創資通

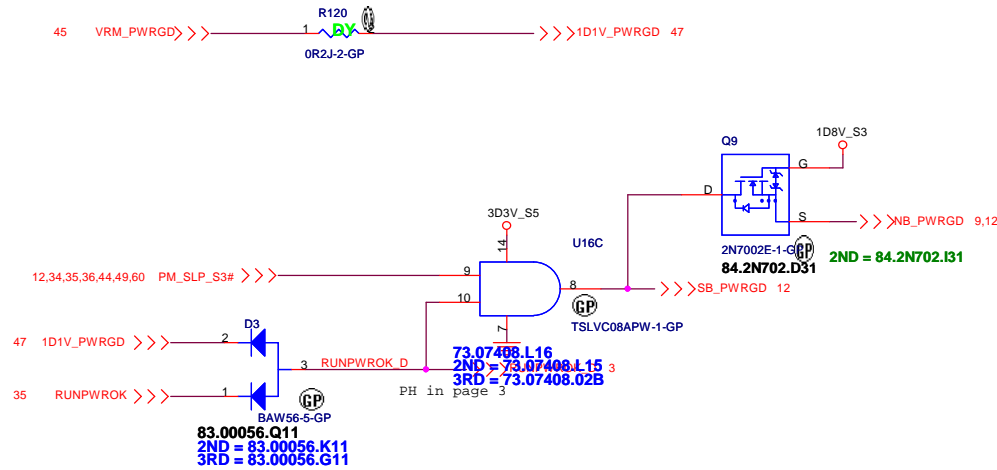
Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title			SWITCH	Rev	SB
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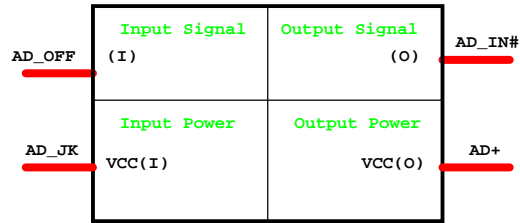


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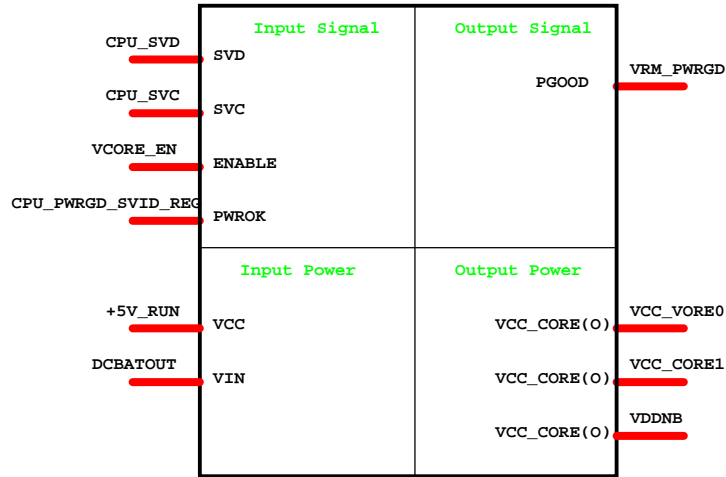
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
POWER ON LOGIC		
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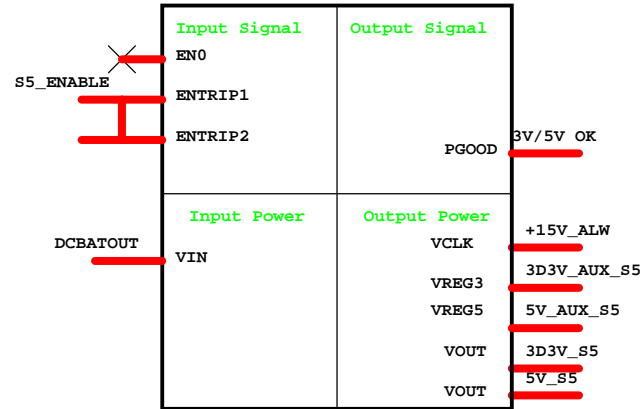
Adapter



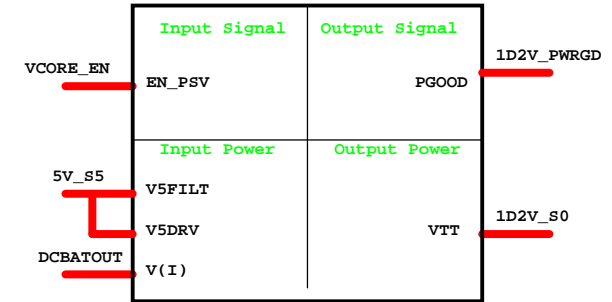
CPU_CORE ISL6265HRTZ



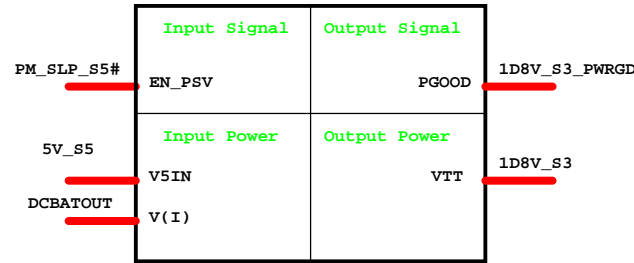
DCDC 5V/3D3V(TPS51125)



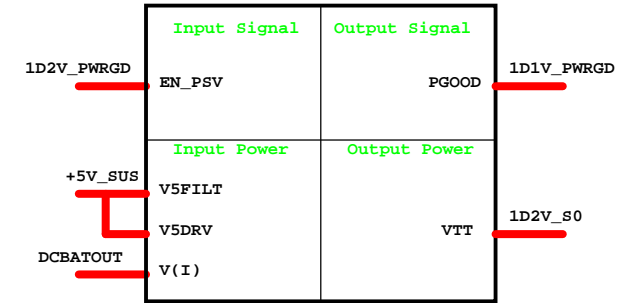
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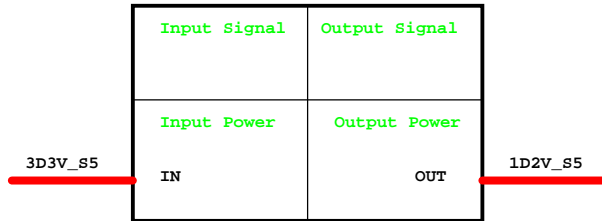
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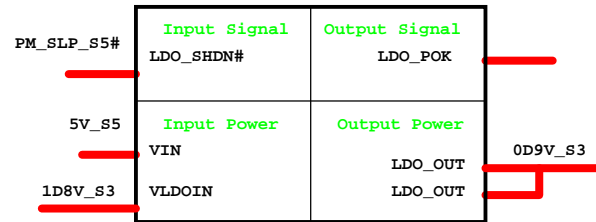
DCDC 1D1V(RT8202)



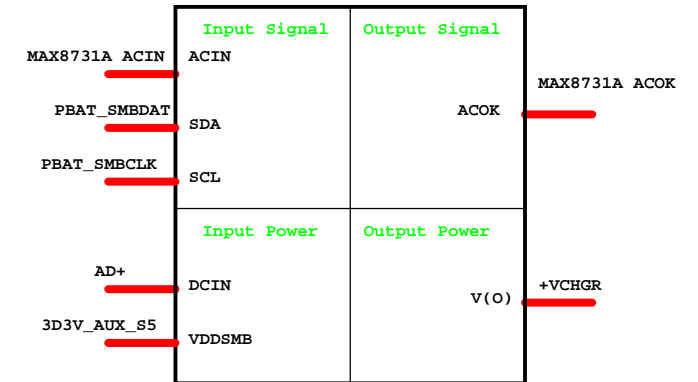
1D2V LDO G9161



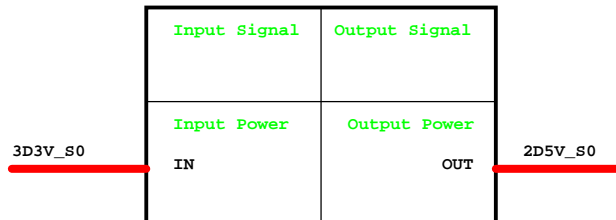
0D9V LDO RT9026



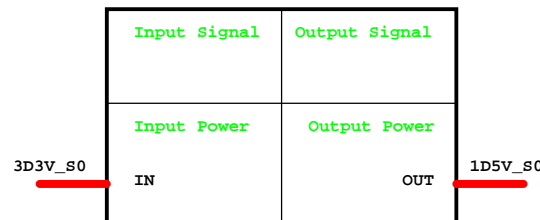
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571



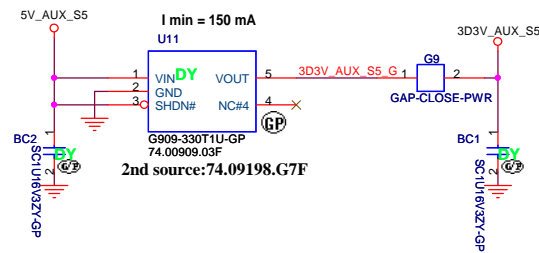
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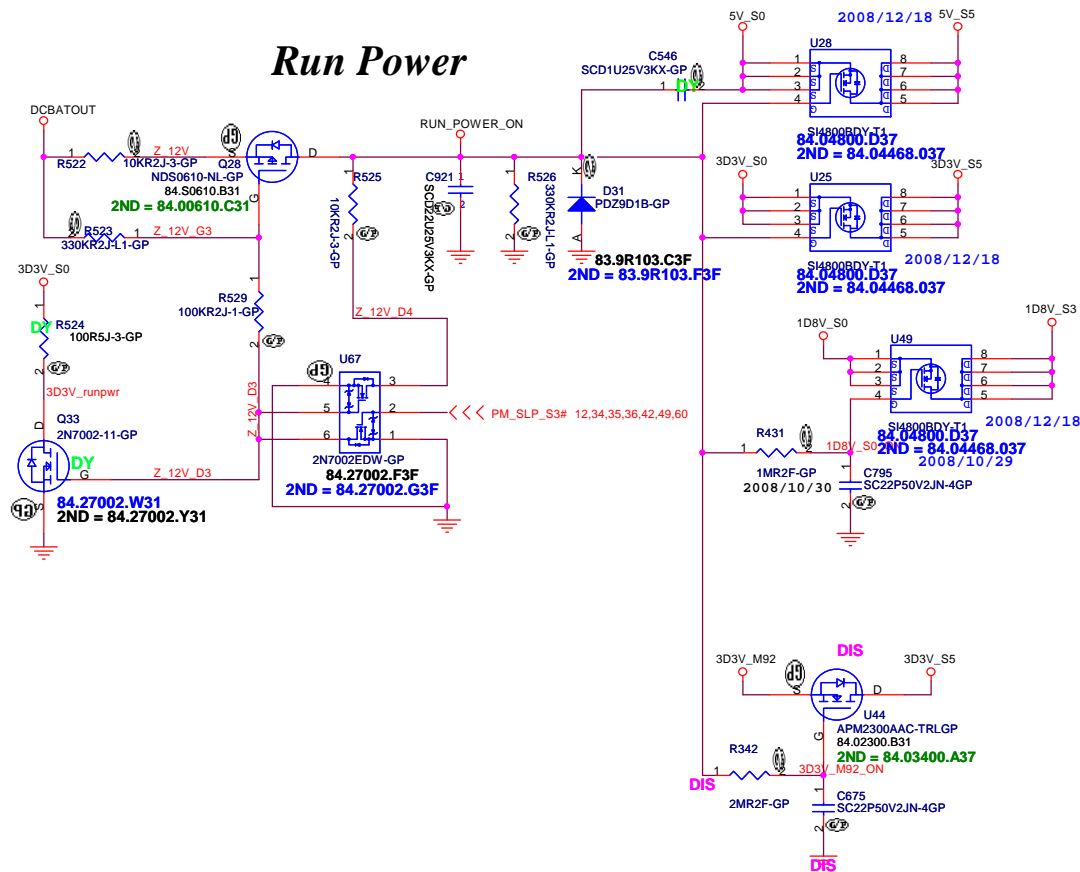
Title			Power Block Diagram		
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Aux Power

3D3V_AUX_S5



Run Power



<Core Design>

緯創資通

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Title	Author	Date	Location	Notes
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RUN AND AUX POWER

Size	A3
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Document Number

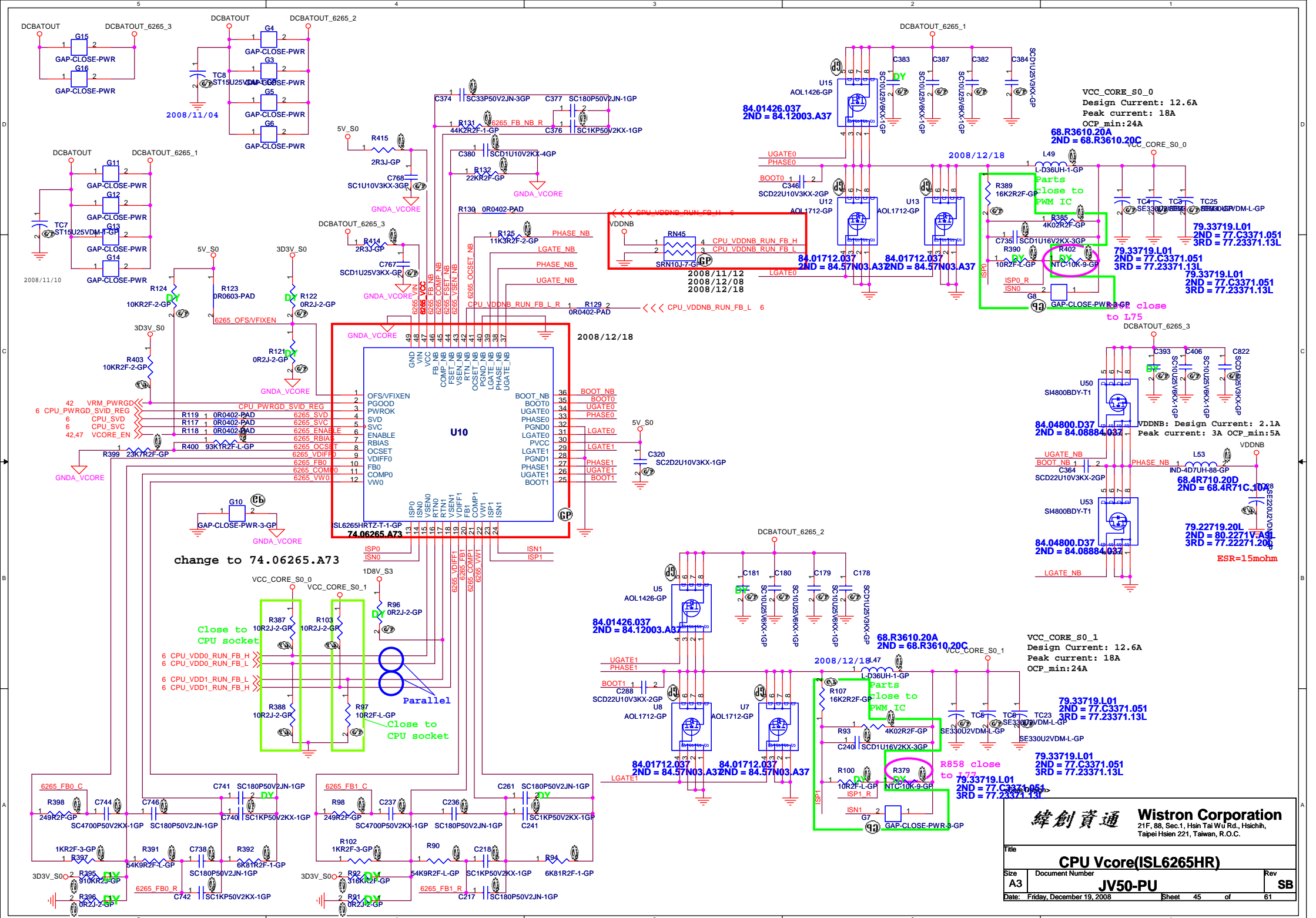
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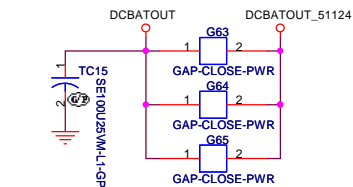
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Date: Friday, December 19, 2008

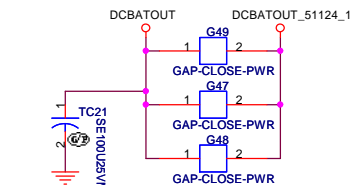
Sheet 44 of

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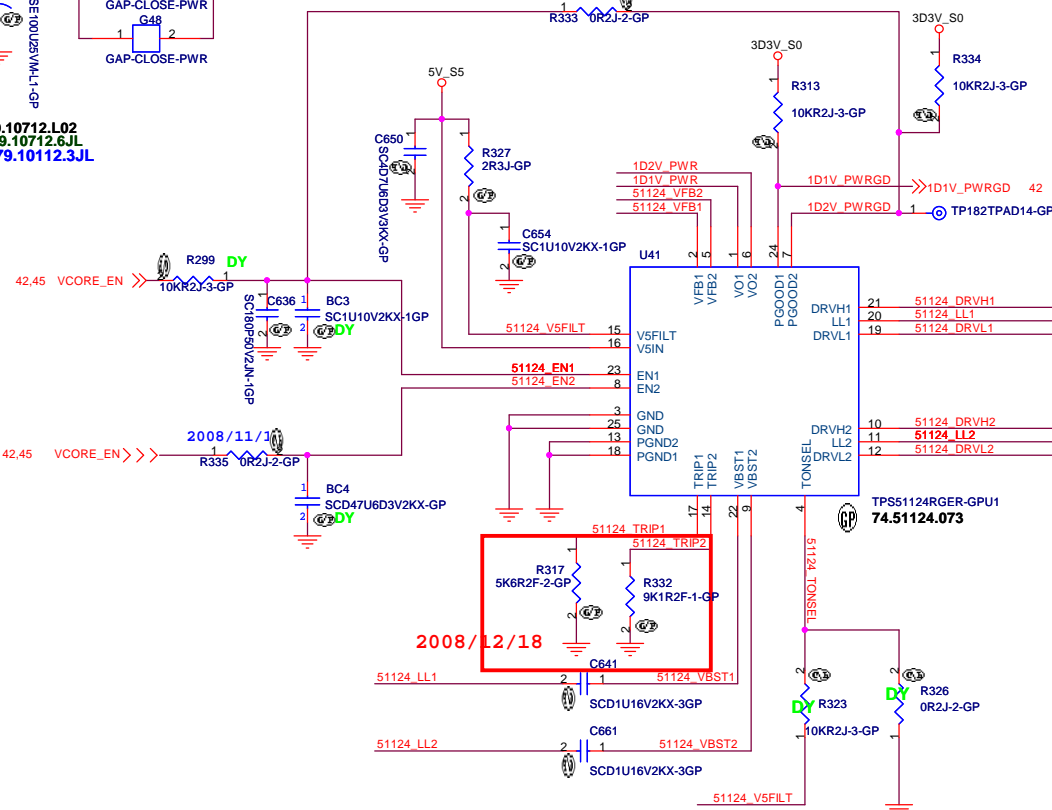
79.10712.L02
2ND = 79.10712.6JL
3RD = 79.10112.3JL



79.10712.L02
2ND = 79.10712.6JL
3RD = 79.10112.3JL

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

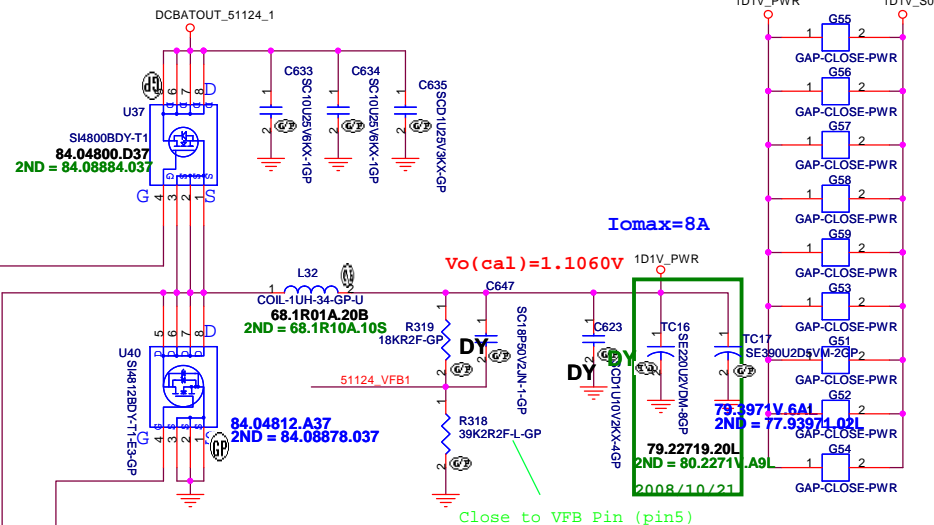
$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$



2008/12/18

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode



20080307_Modify by
Brian
ACOUSTIC NIOSE

84.04812.A37
2ND = 84.08878.037

84.04812.A37
2ND = 84.08878.037

84.04812.A37
2ND = 84.08878.037

84.04812.A37
2ND = 84.08878.037

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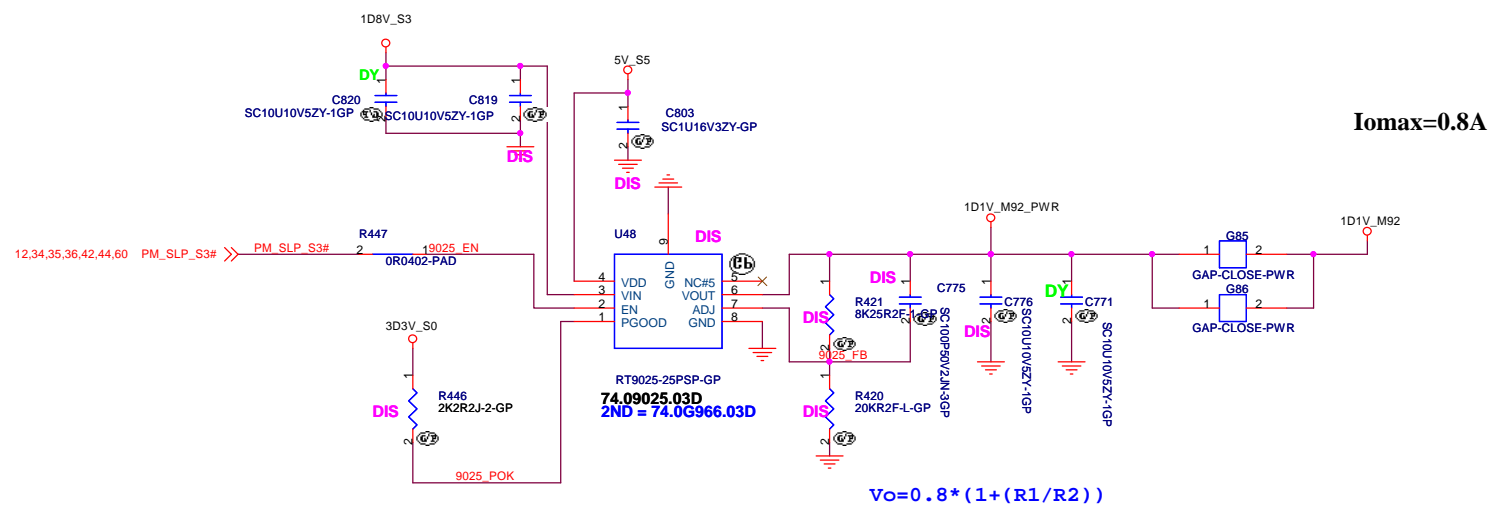
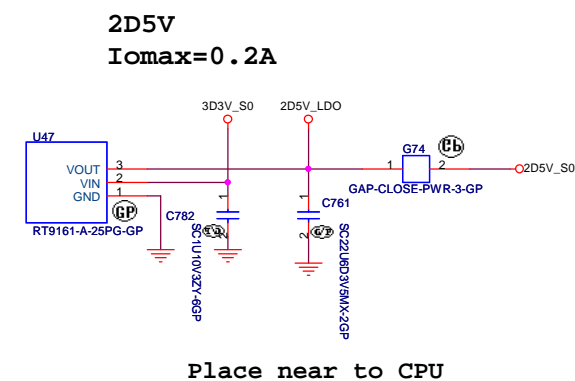
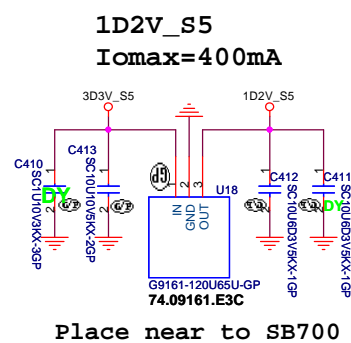
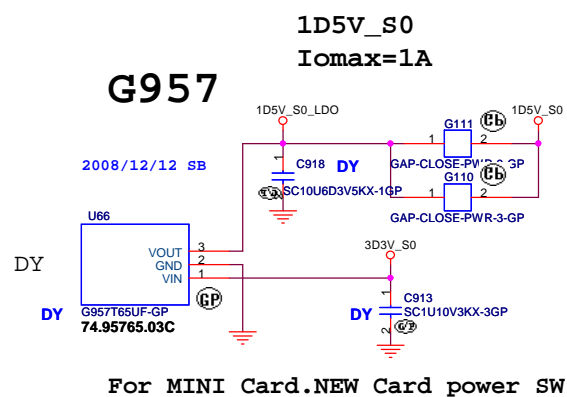
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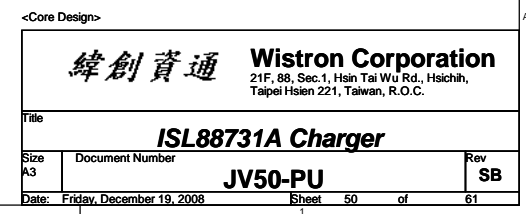
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2ND = 84.08878.037

<Core Design>

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Title	TPS51124 1D1V 1D2V		
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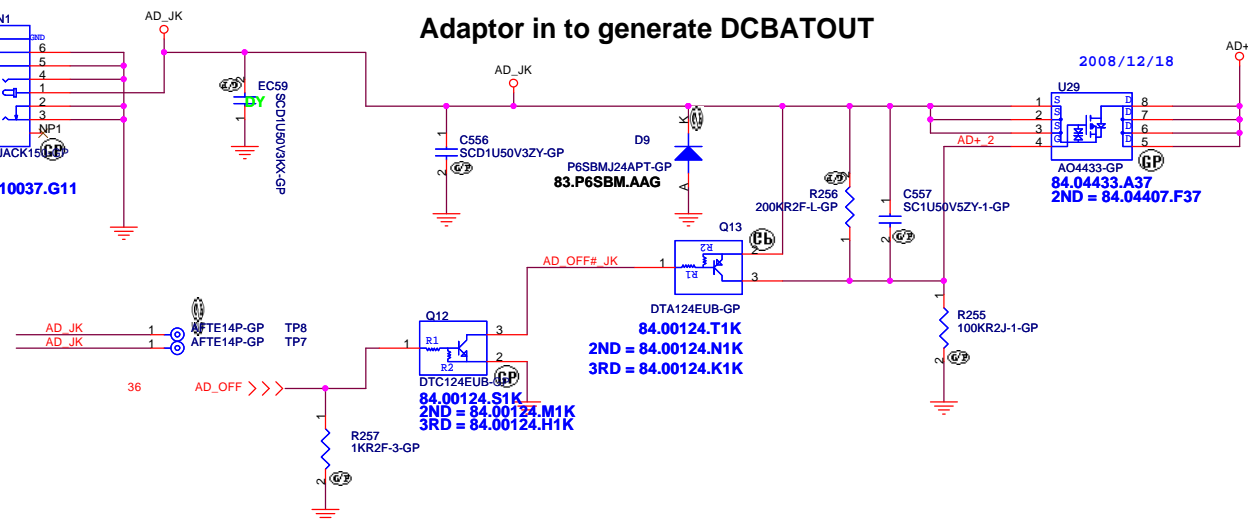
DCIN1

6
5
4
1
2
3
NP1

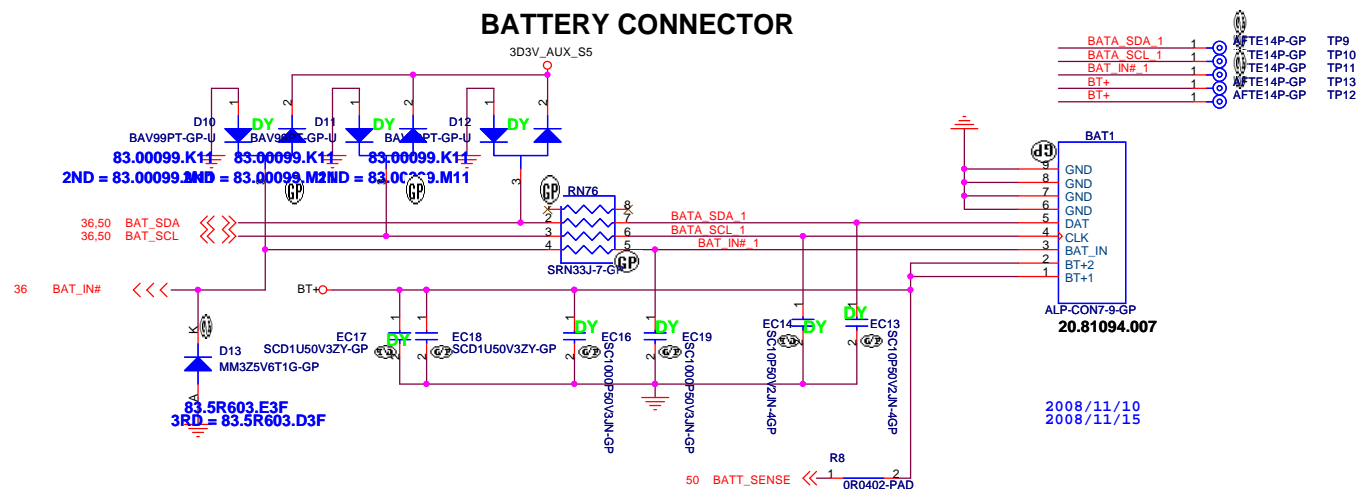
DC-JACK150P

22.10037.G11

Adaptor in to generate DCBATOUT

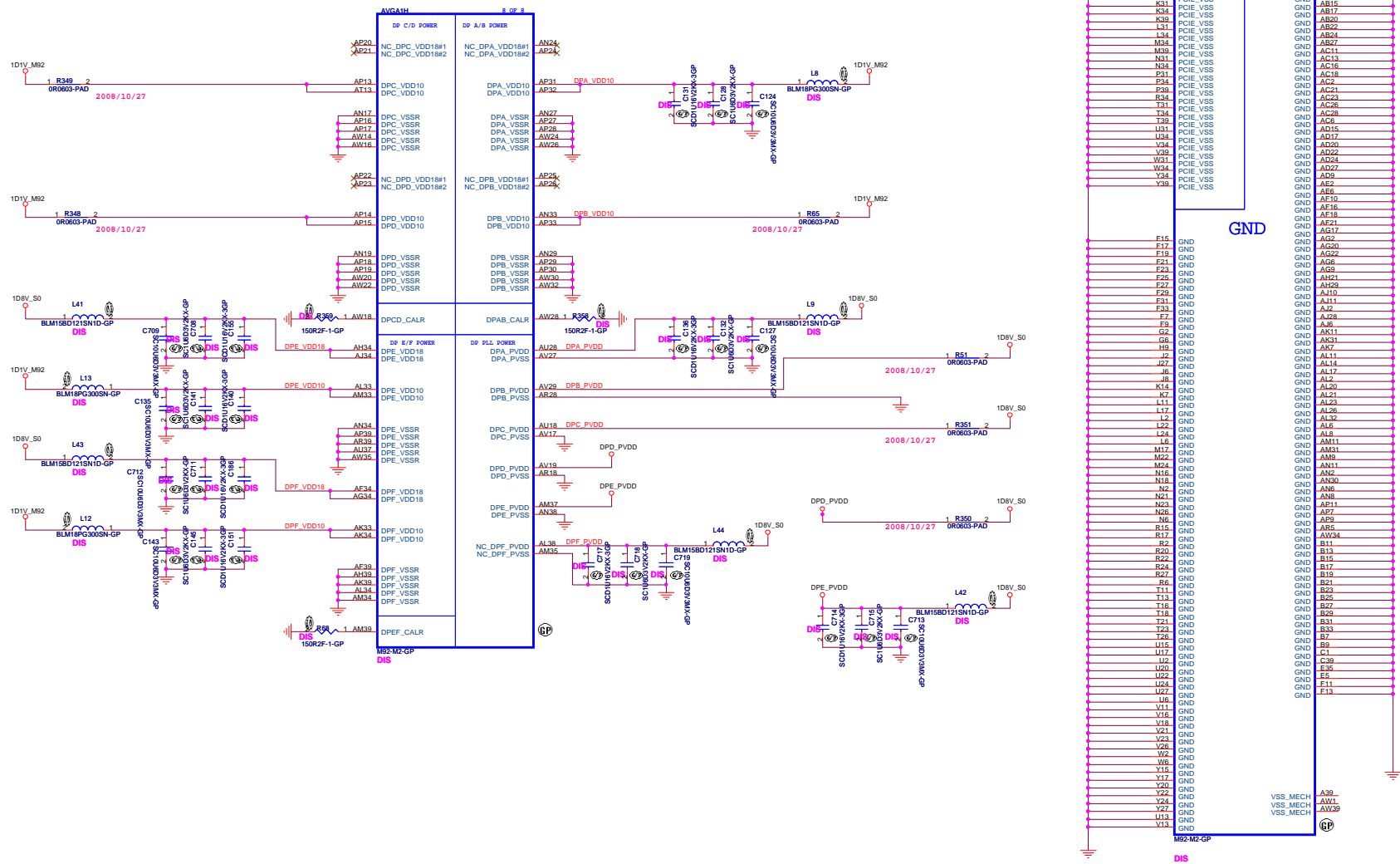


BATTERY CONNECTOR

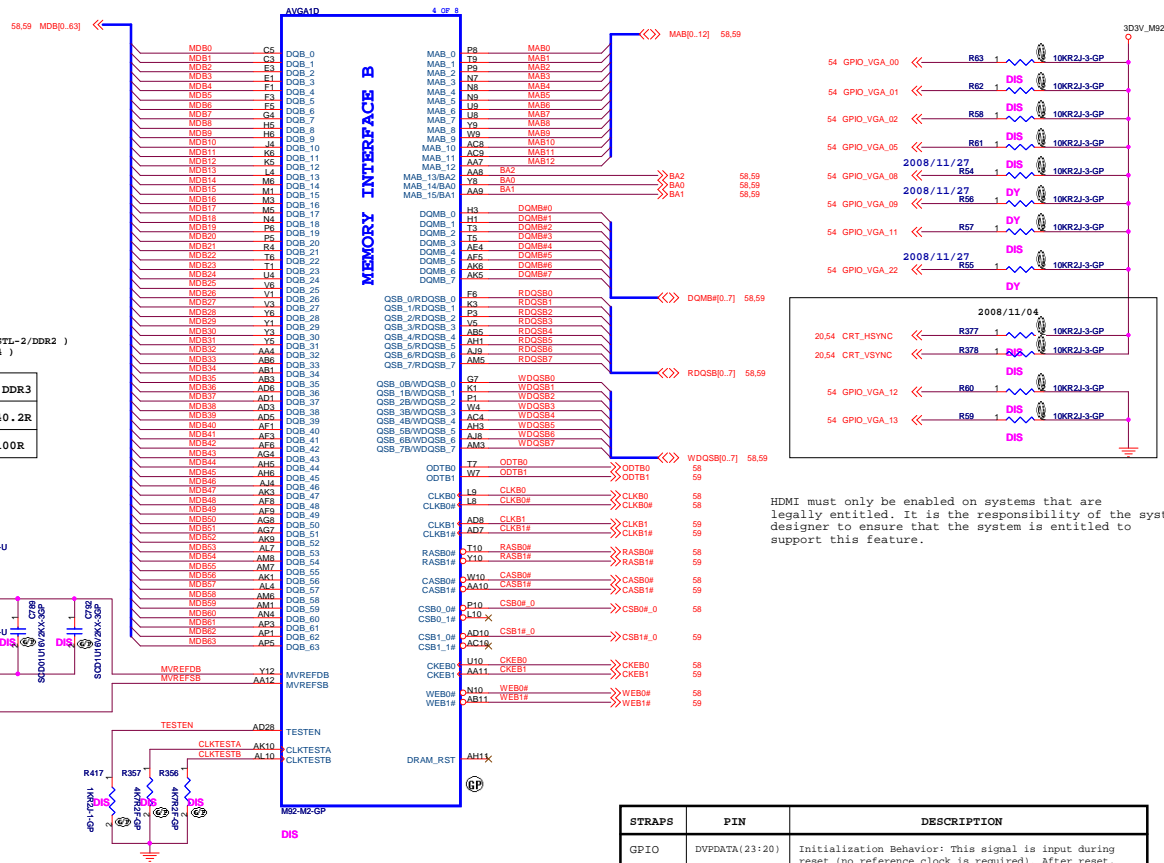


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Title			
AD/BATT CONN			
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M92-M2 uses memory group B only

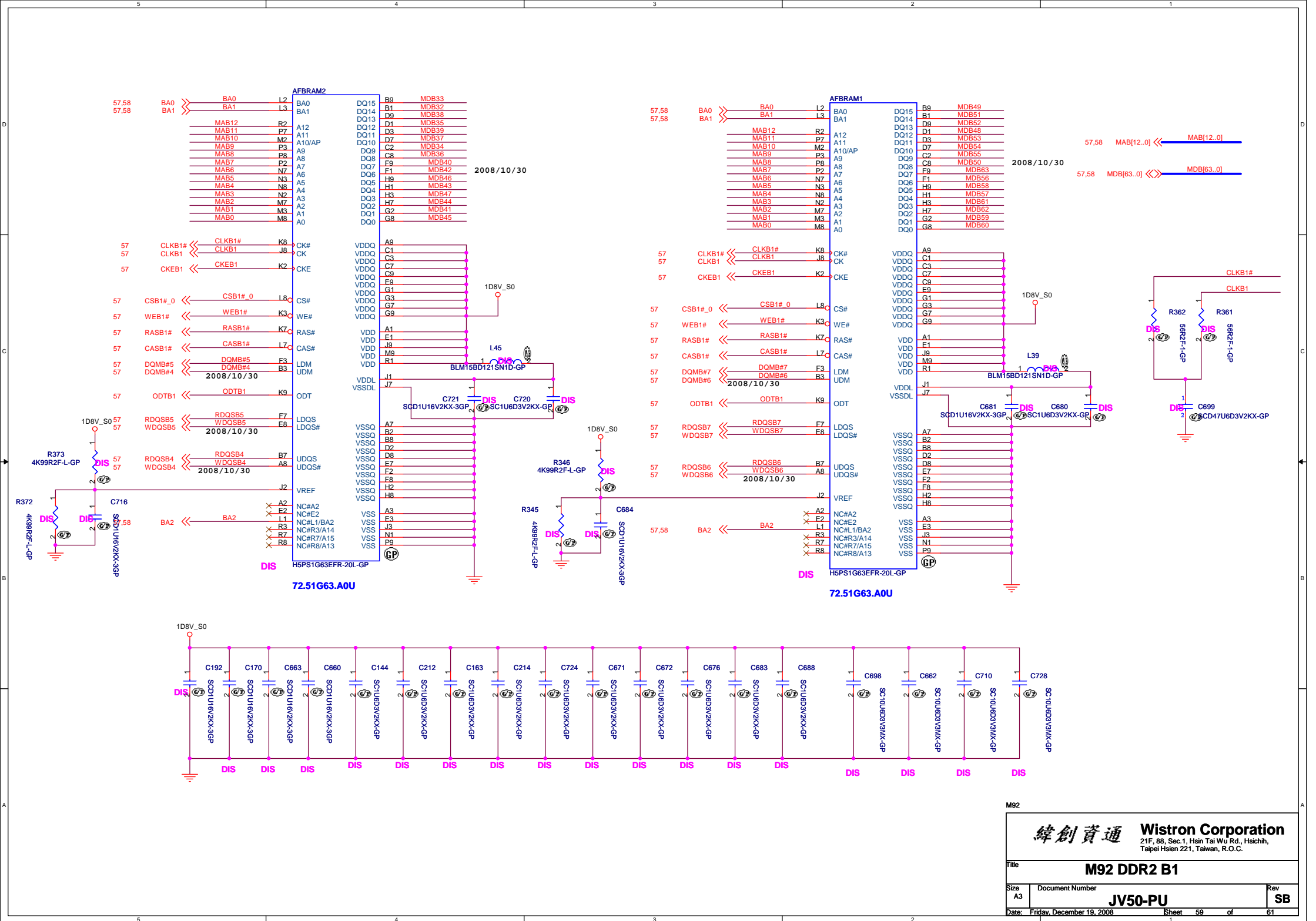


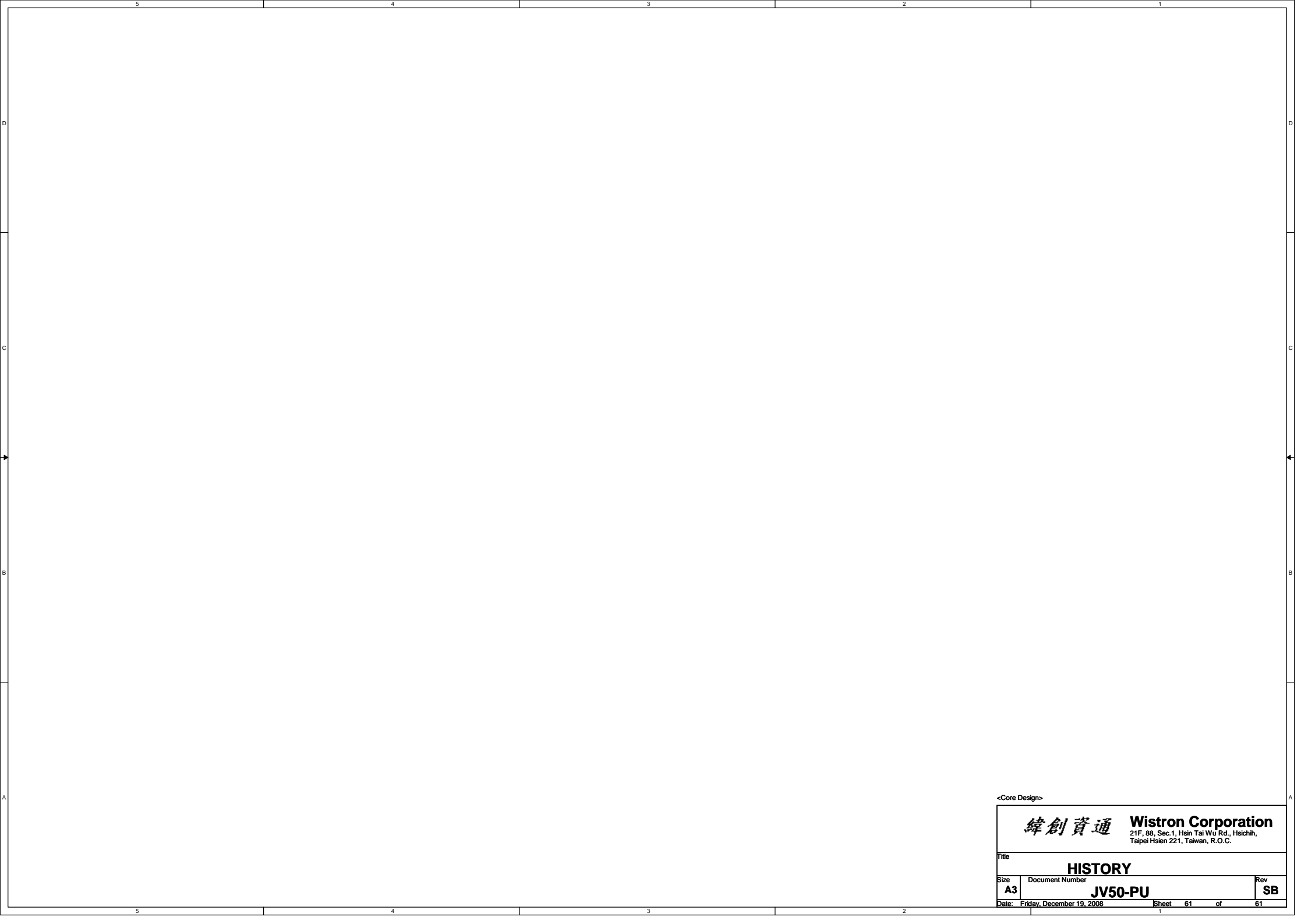
AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC, GENERIC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO, GPIO21_BB_EN	

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly FMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR x= DESIGN DEPENDANT NA= NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50k Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	x x x
PWRCNTL[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	1
CCBPASS	GENERIC		0

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.





<Core Design>

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